Key Testing Considerations for Migrating from Silicon to Silicon Carbide

Webinar 1

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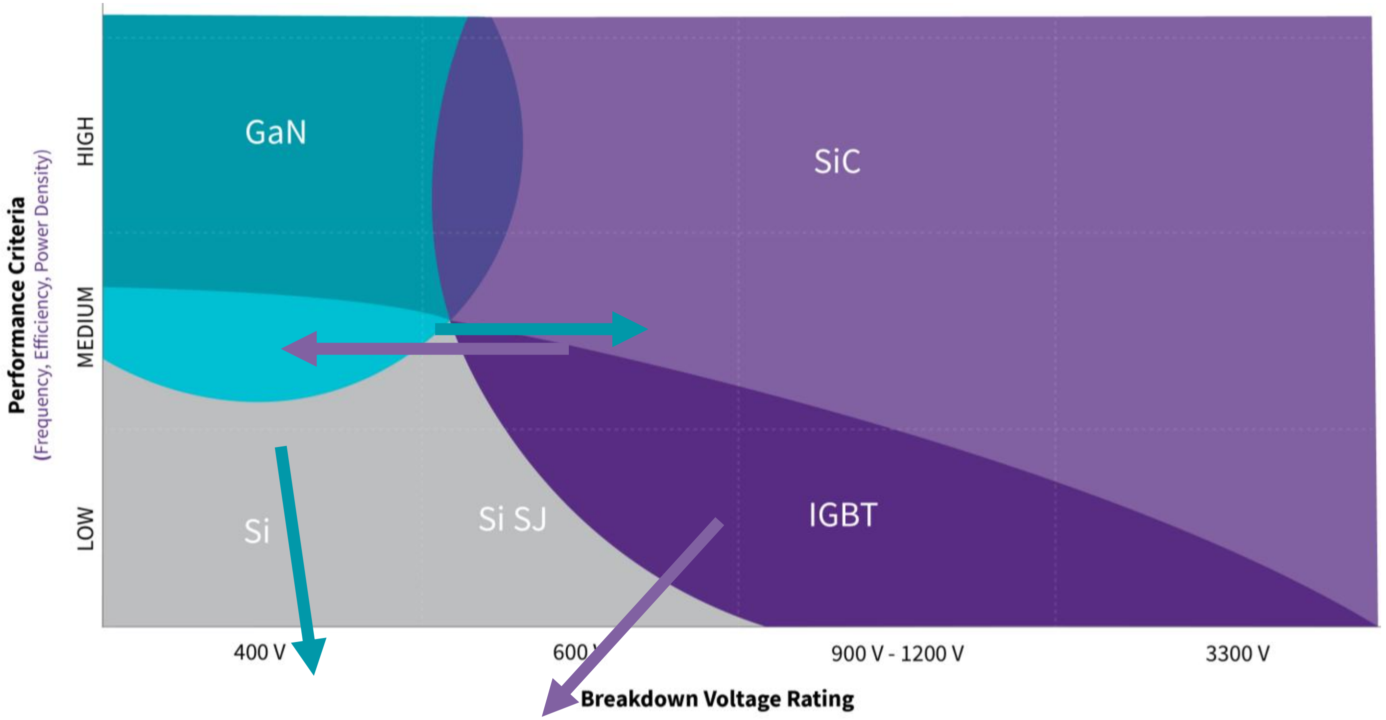
Agenda

1. Why Silicon Carbide (SiC)?
2. SiC Applications
3. SiC Trends
4. Fundamental Measurement Considerations
5. Top Probing Considerations
6. Probing Recommendations
7. Summary
8. Contact Information

Device Technology Landscape



SiC and GaN application space continues to grow and encroach on traditional silicon space

Silicon carbide is the best-in-class technology for power applications from 650 V – 3300 V+

- Lower conduction losses and improved thermal efficiency
- Enables system size reduction
- Reduces system cost

Silicon MOSFETs are highly effective <400V

- 5 V to 650 V devices are common
- Good switching and conduction characteristics
- Not efficient above 650V class

Silicon IGBTs dominate low switch frequency, high power applications today

- 1200V devices dominate motor drive market
- Good power capability up to ~6kHz

GaN is touted for 40 V to 600 V

- High switching frequency, high power density
- Lower current & power: Generally several kW max

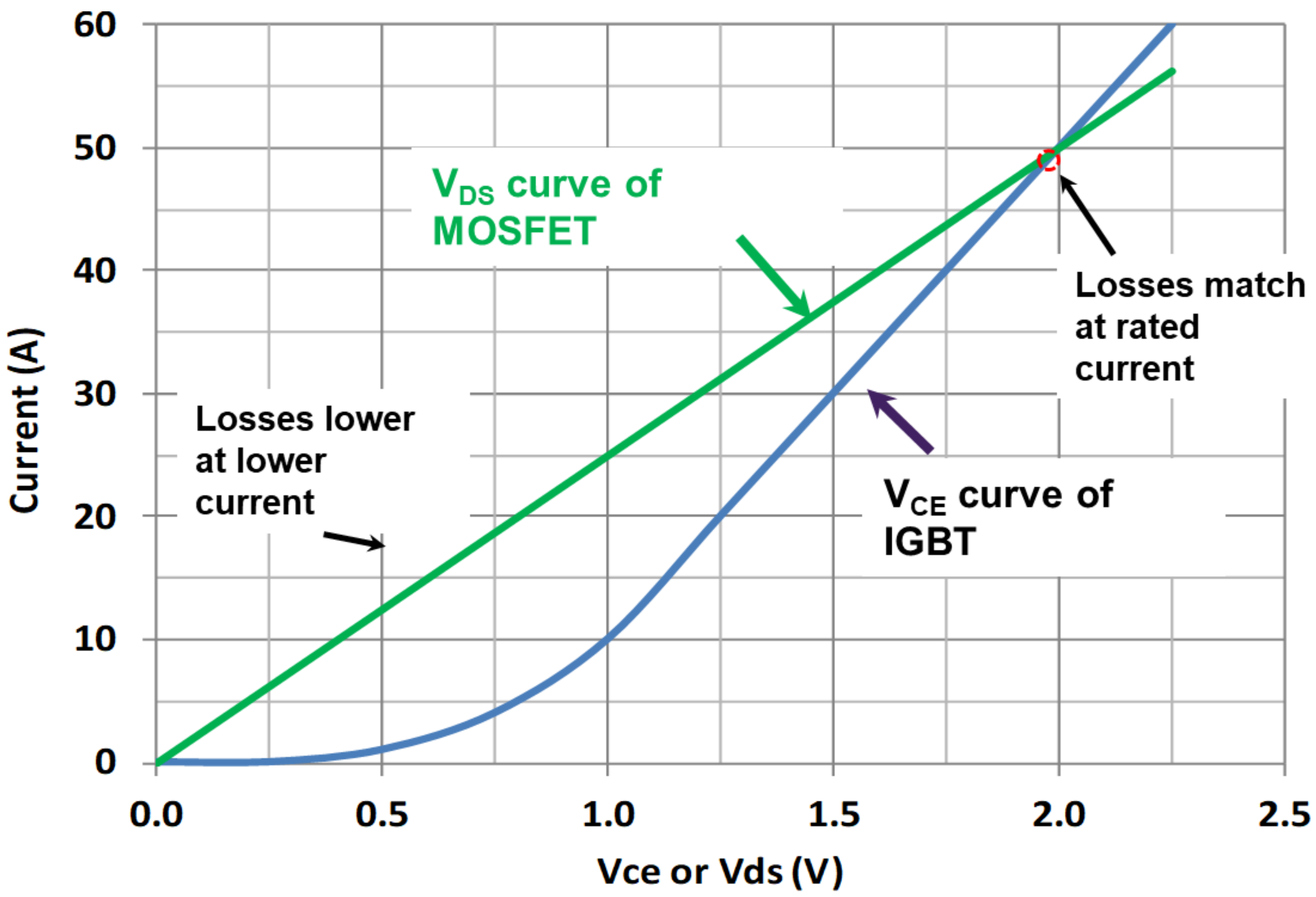
Why SiC?

Why SiC?

- Smaller capacitance → Fast switching and low switching losses
- Less temperature dependence of $R_{DS(on)}$ compared to Si MOSFET
- Low reverse recovery body diode enables reliability in hard-switching applications
- Enables high-frequency hard-switching applications such as totem-pole PFC and 3-phase active front ends
    - ✓ Enabling higher switching frequency
    - ✓ Increasing power density and reducing weight
    - ✓ System cost savings
    - ✓ High efficiency
    - ✓ Bi-directional operation
    - ✓ Proven technology with trillions of field hours

1200V SiC MOSFET vs. Si IGBT

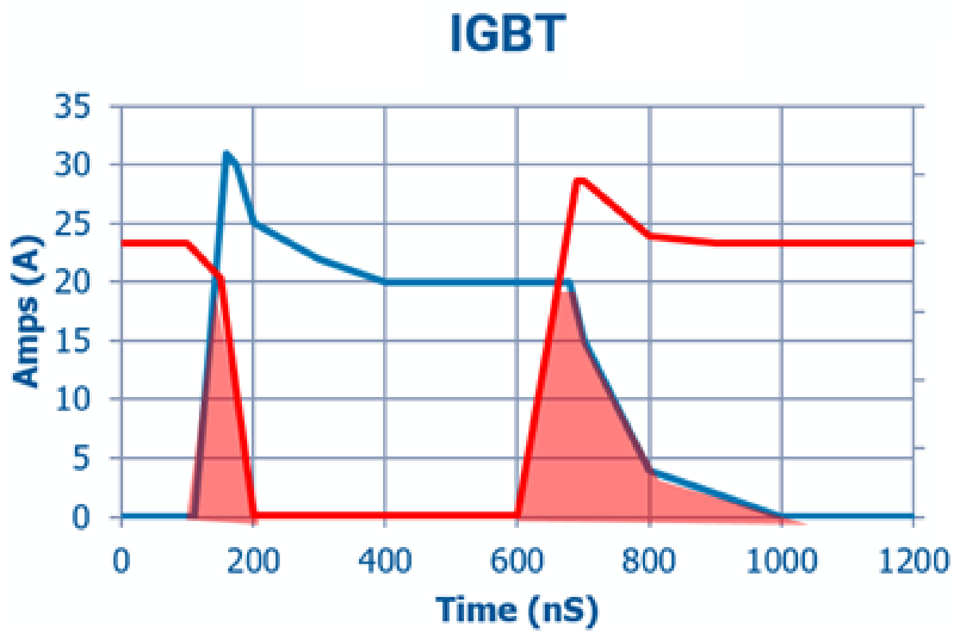
CONDUCTION LOSS

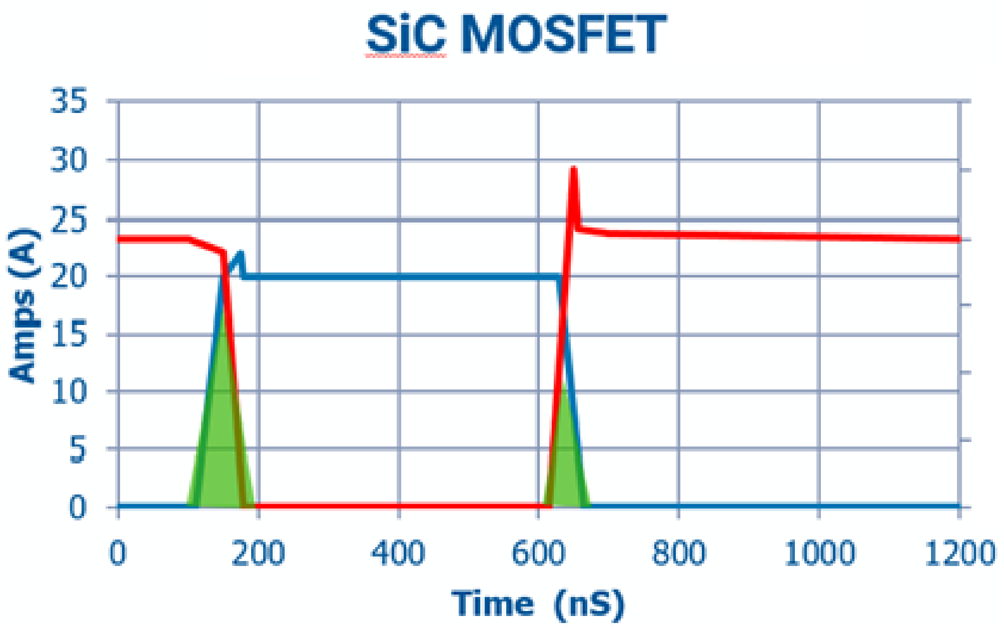


- Comparison of 40A IGBT to 40A SiC MOSFET
- SiC MOSFETs have lower conduction losses than IGBT from 99% rated current and below
- Light and medium load efficiency is greatly improved with SiC for both hard and soft switching applications

1200V SiC MOSFET vs. Si IGBT

SWITCHING LOSS





- IGBT tail current impacts the turn-off loss
- Eoff=2.66mJ
- Etotal=Eon+Eoff=4.86 mJ

- IGBT tail current eliminated with SiC
- Eoff=0.1mJ
- Etotal=Eon+Eoff=0.71mJ

➢~95% lower turn-off switching losses! – applicable for soft switching

➢~85% lower total switching losses! – applicable for hard switching

SiC Applications

SiC Power Applications

Automotive

- On-Board Charging
- On-Board Dc-Dc
- Drivetrain
- Off-board Charging

Energy

- Solar Inverters
- Energy Storage
- Smart Grid
- Wind

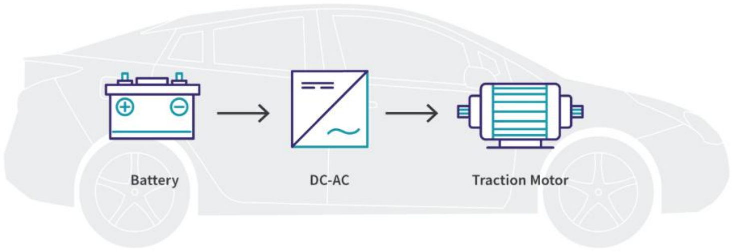
Light Industrial

- Server SMPS
- AI Datacenter
- Aux Power
- Medical

Heavy Industrial

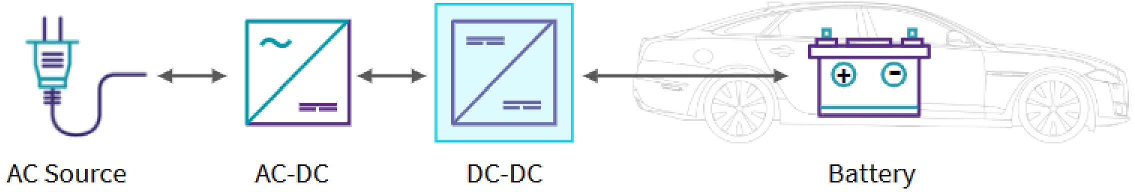
- Traction
- Welding
- Induction Heating
- Industrial Robots

Automotive Electrification



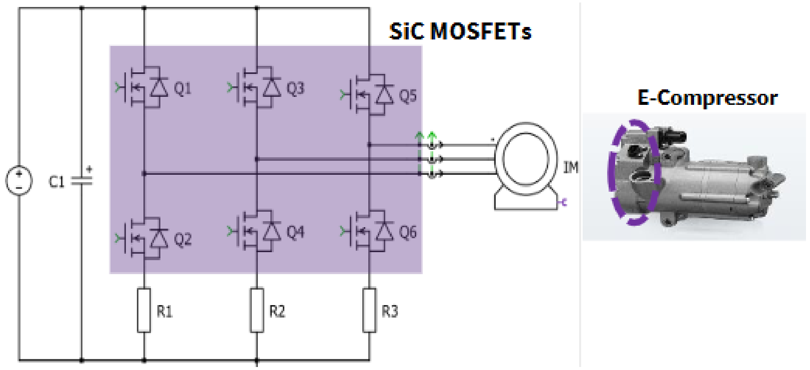
Traction Inverters

Largest single application of SiC devices



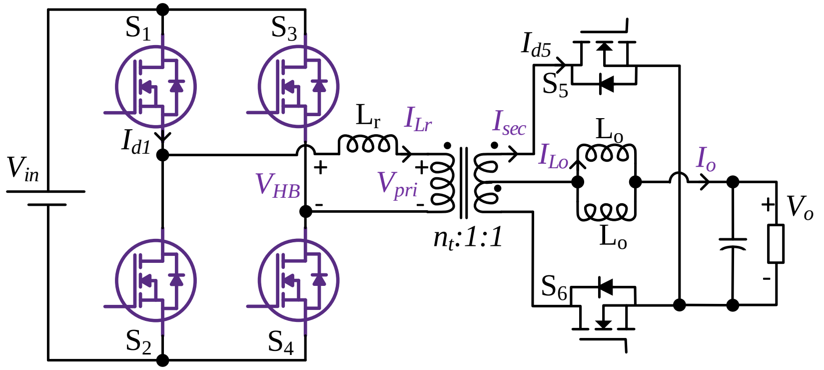
Charging

On-board and off-board fast charging



HVAC and Auxiliary Motors

More efficient heat pumps



HV → LV Power Supply

400/800V battery to 12-48V system

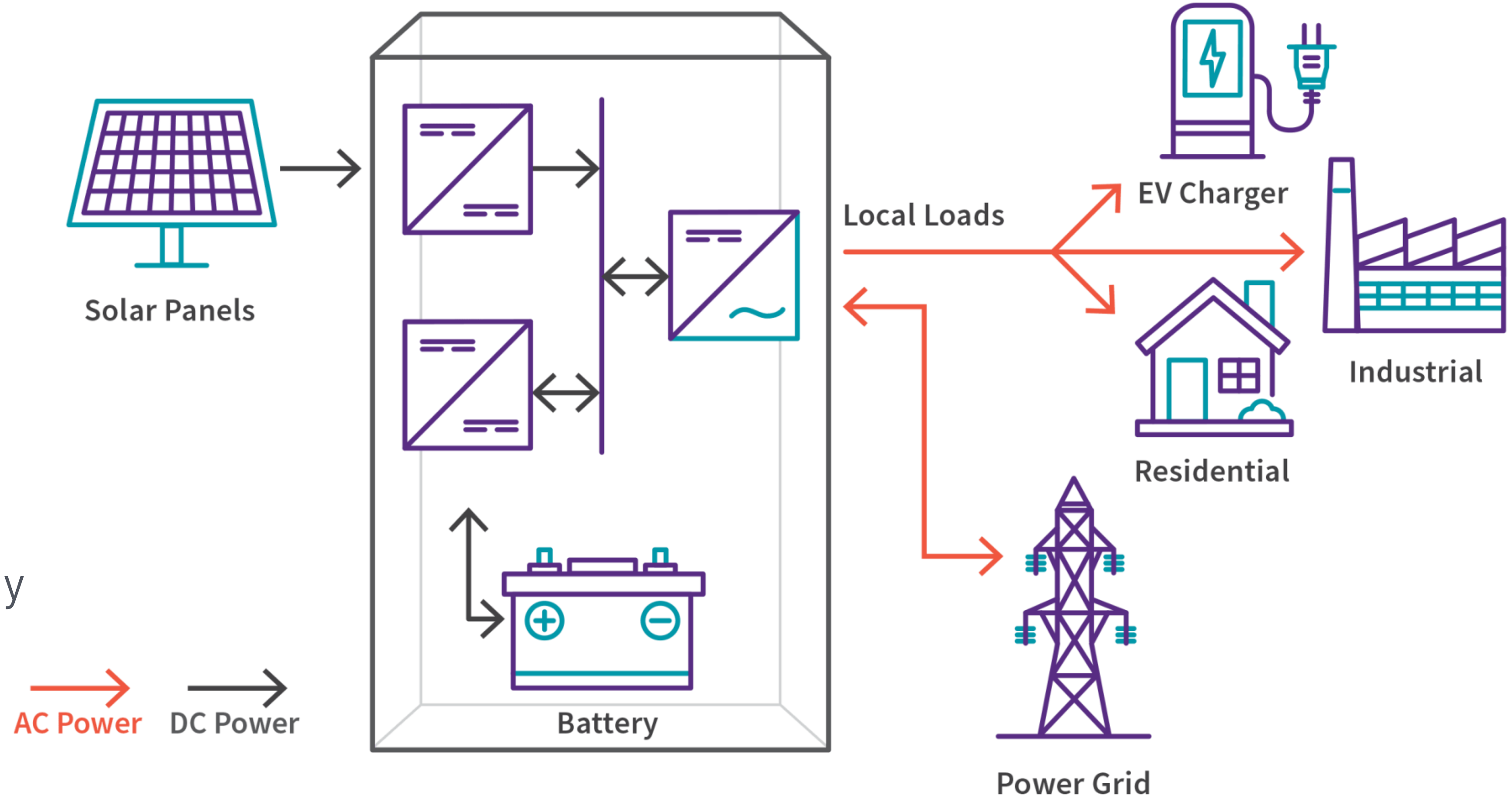
Energy: Solar & Energy Storage

System Elements

Maximum Power Point Tracking (MPPT) boost

DC-AC Inverter

Non-isolated DC-DC energy storage interface

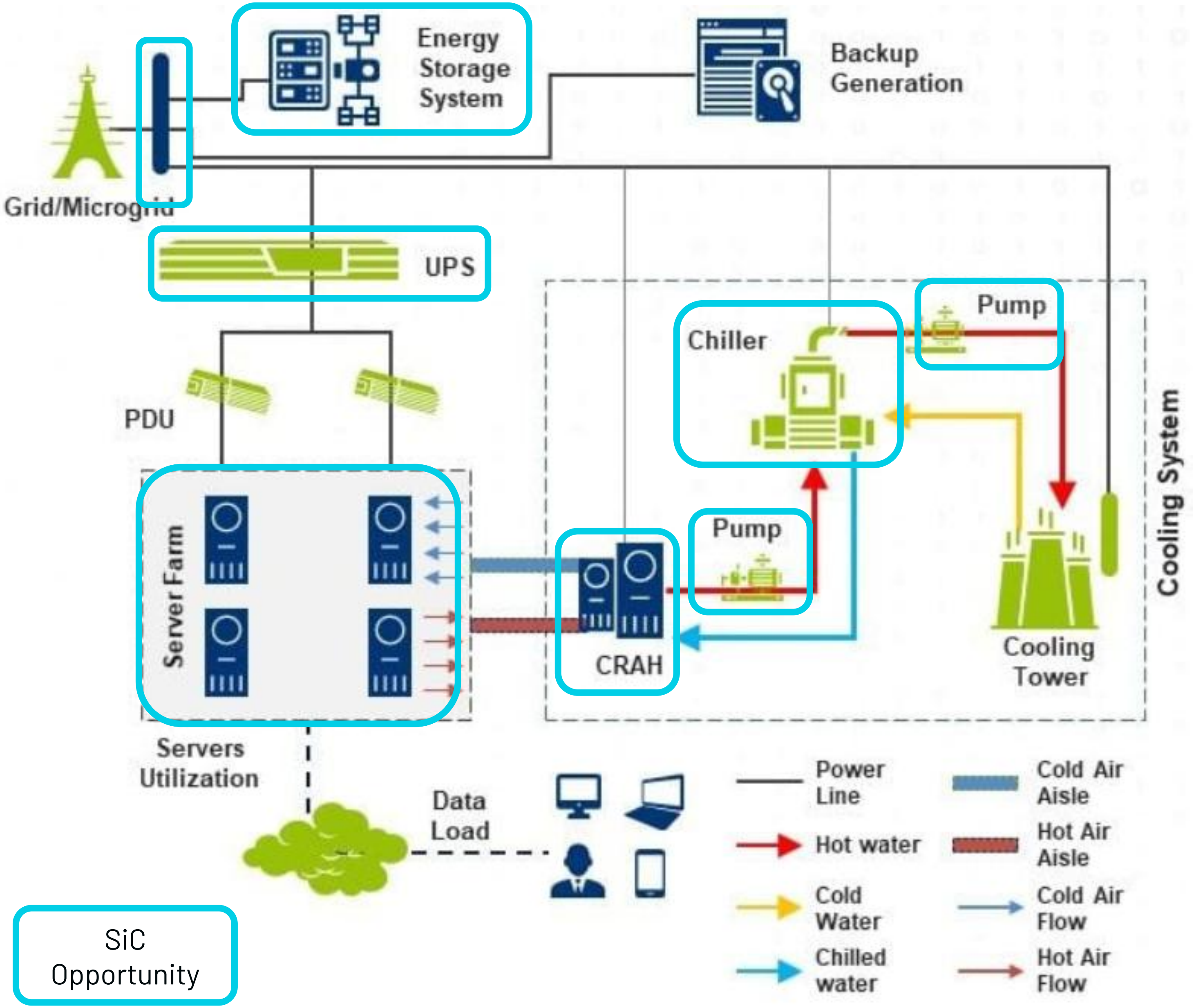


Data Center

- SiC is currently utilized primarily in energy storage system, UPS and AC/DC rack power supplies

- Emerging opportunities in HVAC components including chillers, pumps, and air handlers

- Solid-state transformers (SSTs) to interface with MV grid are in development to improve power quality and efficiency



Industrial Motor Drives

Early Adopters

Air Core Motors

60-100kHz switching frequency required

Servo Motors

High switching frequency and power density

Emerging

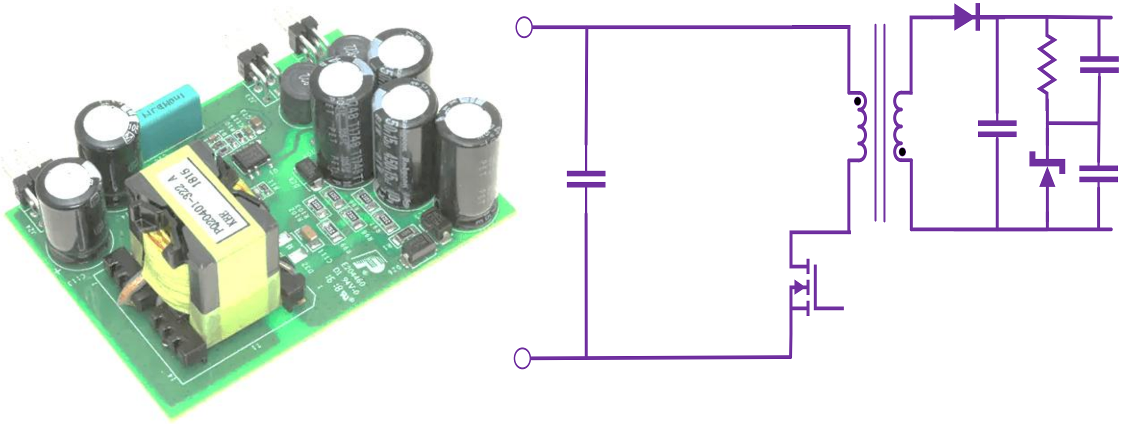
HVAC & Integrated Motor-Drives

High efficiency requirements and cost savings

General Purpose Merchant Drives

Low switching frequency, cost driven application

Auxiliary Power Supplies



Integrated in Systems

10-200W supplies for control and cooling

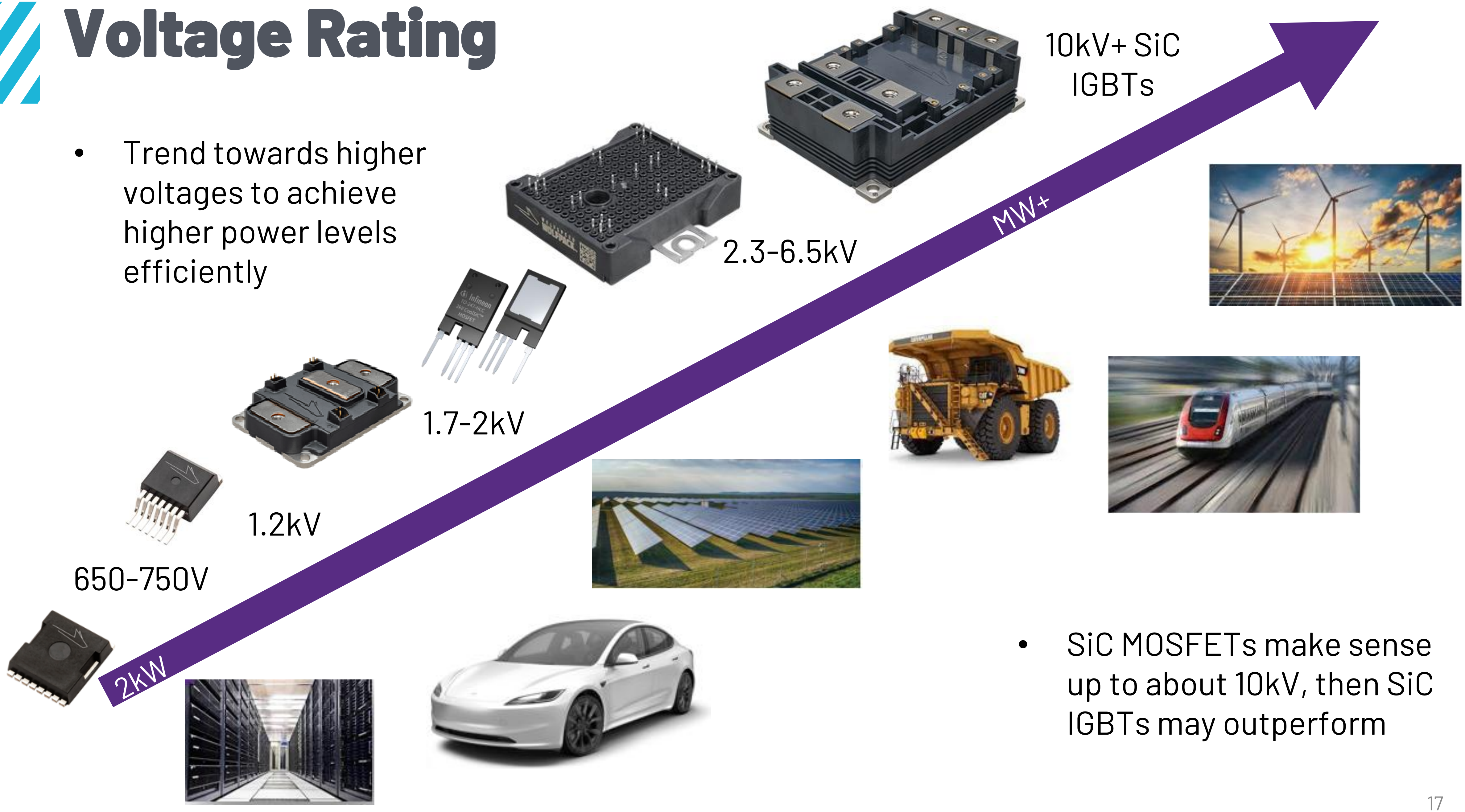
Stand-Alone Power Supplies

DIN and rack power supplies for control

SiC Trends

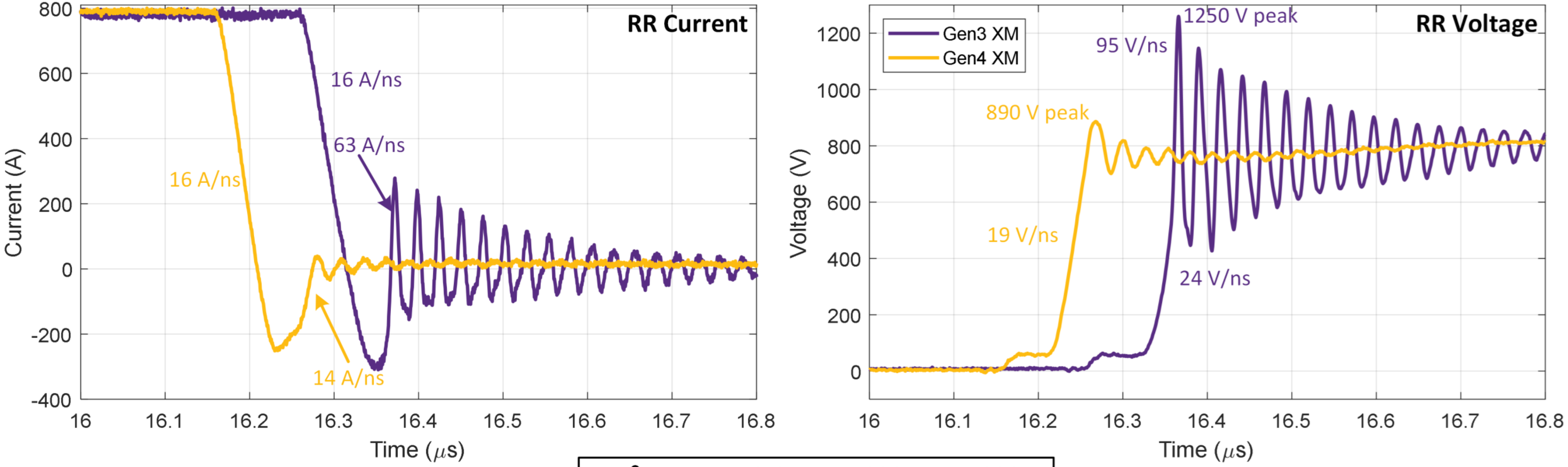
Voltage Rating

- Trend towards higher voltages to achieve higher power levels efficiently



- SiC MOSFETs make sense up to about 10kV, then SiC IGBTs may outperform

Wolfspeed Gen 3 vs. Gen 4 – Soft Body Diode



175°C, $R_{G\text{-}EXT}$ = 0 Ω, V_{DS} = 800 V, I_S = 800 A

- Reduced snappiness in Gen 4 body diode yields significantly lower voltage overshoot
- This allows operation at lower gate resistance and thus lower switching losses

Fundamental Measurement Considerations

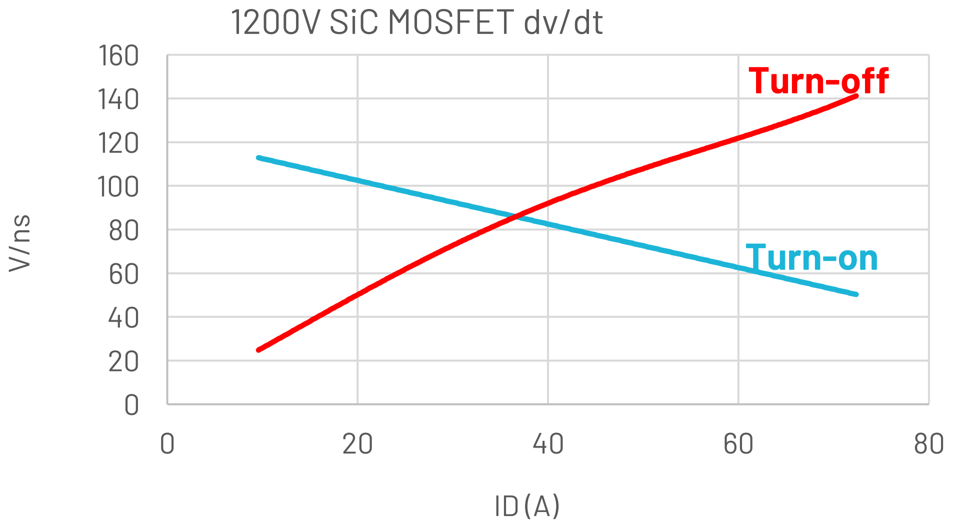
Bandwidth

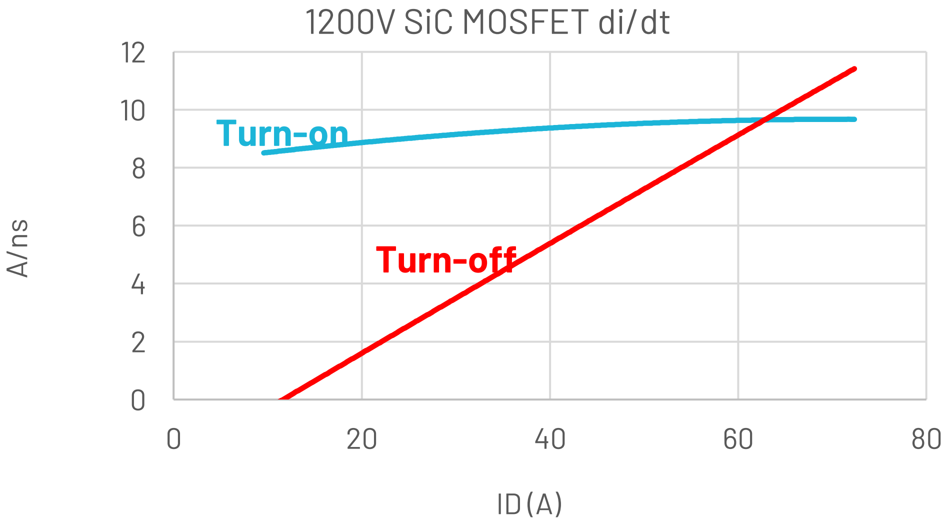
Silicon Carbide MOSFETs can easily generate dv/dt in excess of 100 V/ns, and di/dt over 10 A/ns

- A 400 V switching transient may only last 4 ns
- The signal bandwidth can be approximated using the equation:

$$BW(MHz) = \frac{350}{Rise\_Time(ns)} \rightarrow \frac{350}{4ns} = 87.5\ MHz$$

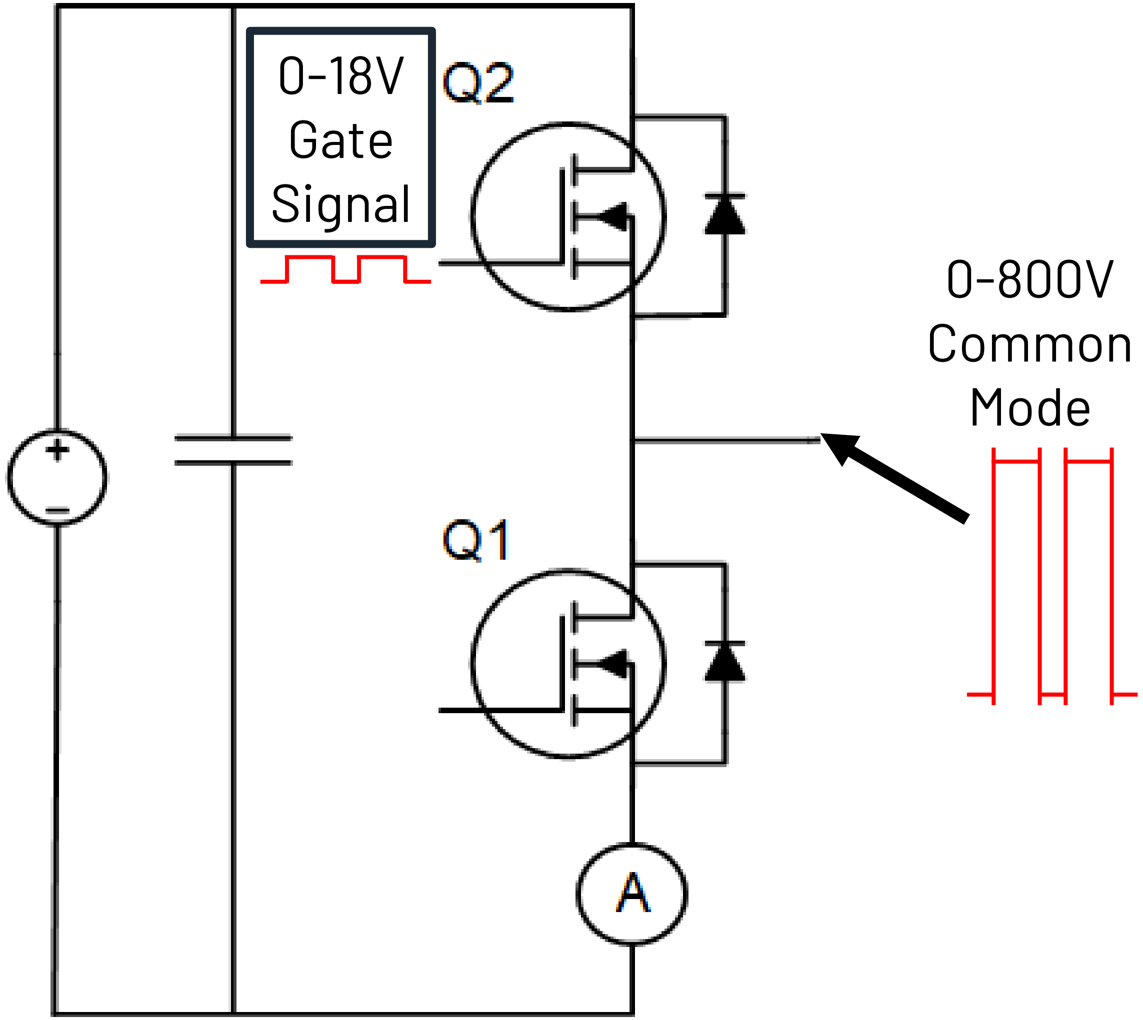
Select a scope and probes with at least 5X the bandwidth of the measured signal. → 500 MHz minimum





Common Mode Rejection

- Parasitic capacitances in the circuit, probe, and oscilloscope provide a high-frequency path that can distort signals
- Isolated probes with high CMRR improve signal fidelity
  - Critical for precise measurements
- Small signals riding on large common-mode signals are especially sensitive – i.e. Gate Voltage

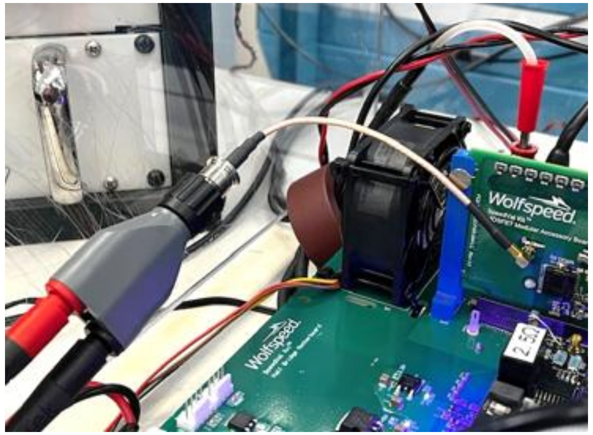


Probe Specification Comparison

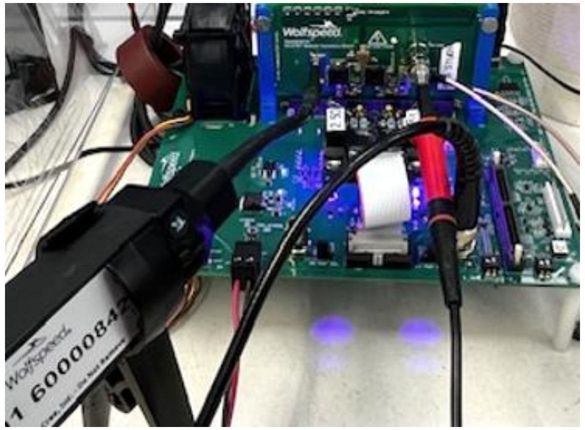
High Voltage
Differential Probe

	HV Differential Probe	IsoVu Fiber Optic Probe
Brand	Tektronix	Tektronix
Model	THDP0200	TIVP1 + MMCX TIP
Bandwidth	200MHz	1GHz
CMRR	DC: >80 dB 100 MHz: >26 dB	DC: >160 dB 100 MHz: >120dB

IsoVu Fiber Optic
Isolated Probe

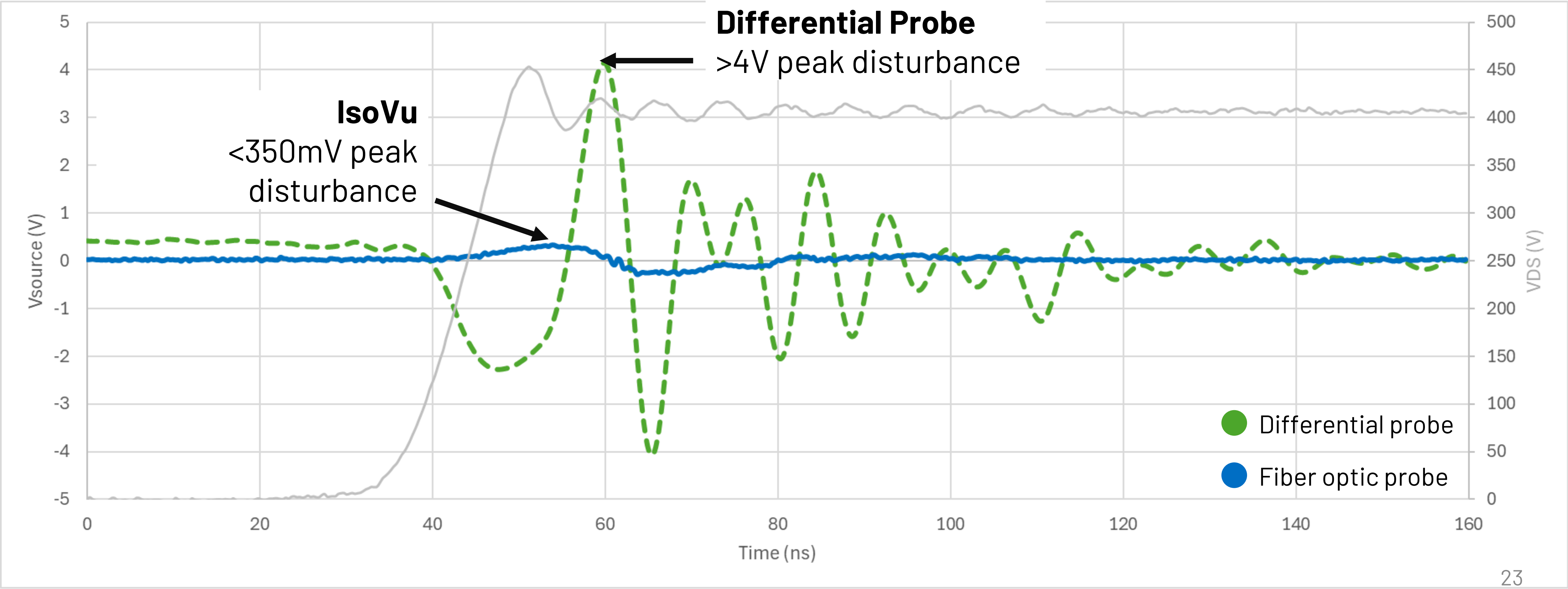


The differential probe is converted to an MMCX plug using an adapter to provide the best signal shielding



Testing the Common Mode Rejection Performance in the Application

- Connect both the tip and reference/ground lead of the probe to the same point in the circuit
- Any signal coming through is due to common-mode noise as the result should be 0V

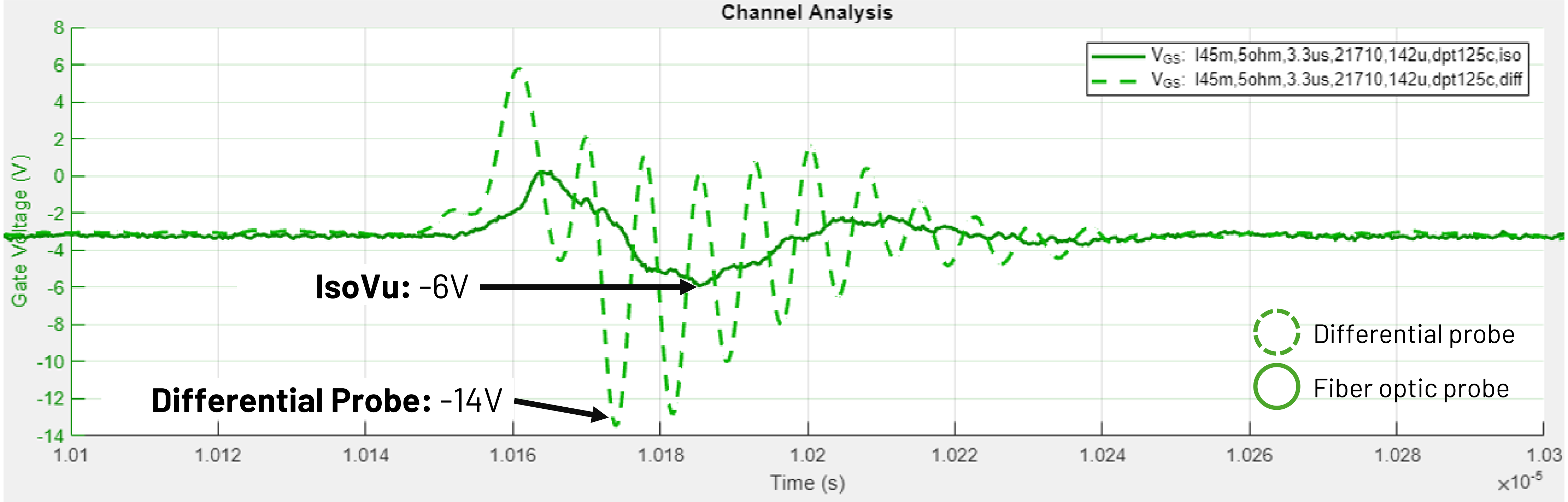


Differential Probe
>4V peak disturbance

IsoVu
<350mV peak disturbance

Why It Matters

- Potential to waste time, effort and money solving a problem that doesn't exist
- Example showing high-side MOSFET VGS while the low-side MOSFET switches on
- Differential probe shows -14V peak which would violate the MOSFET absolute maximum ratings
- Actual worst-case shown by IsoVu is only -6V, comfortably within SOA → No issues



IsoVu: -6V

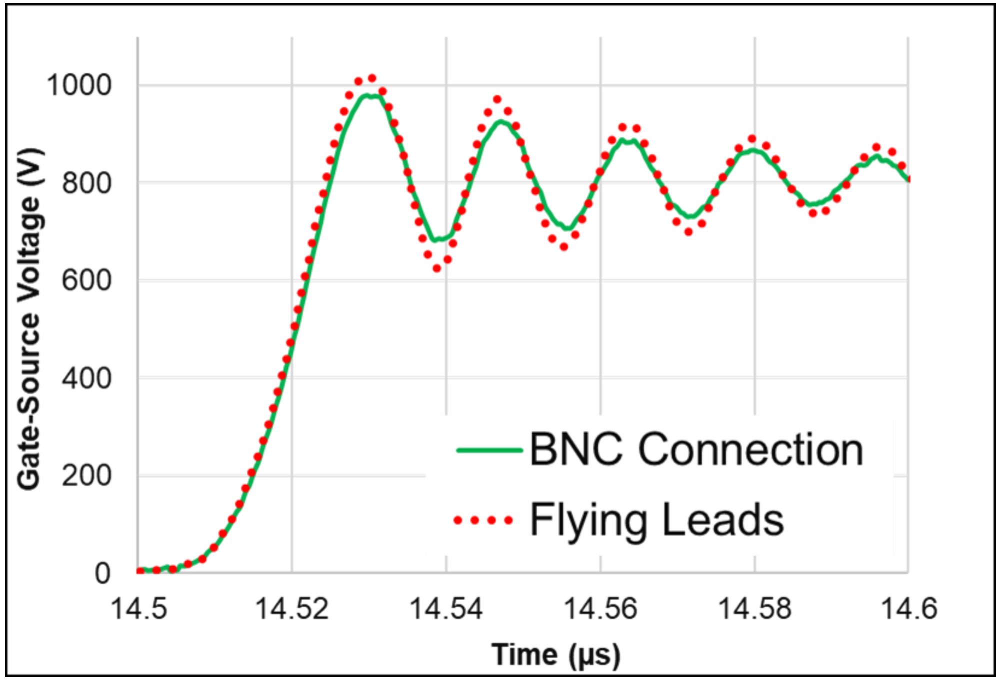
Differential Probe: -14V

Differential probe

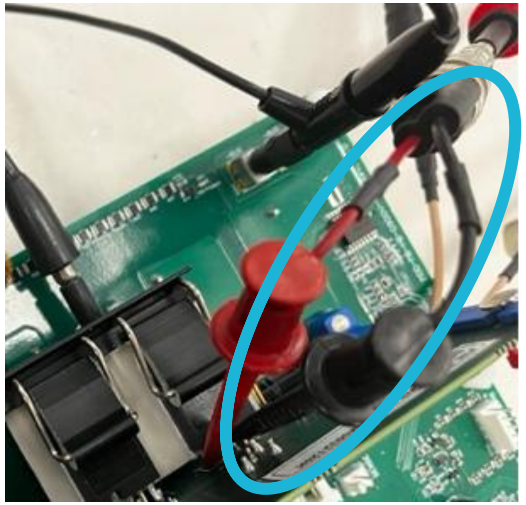
Fiber optic probe

Probe Connections

- Differential noise can couple into the probe and distort signals
- Use a coaxial connection if possible – BNC works up to 500 V
- Minimize loop area when using differential or passive probes



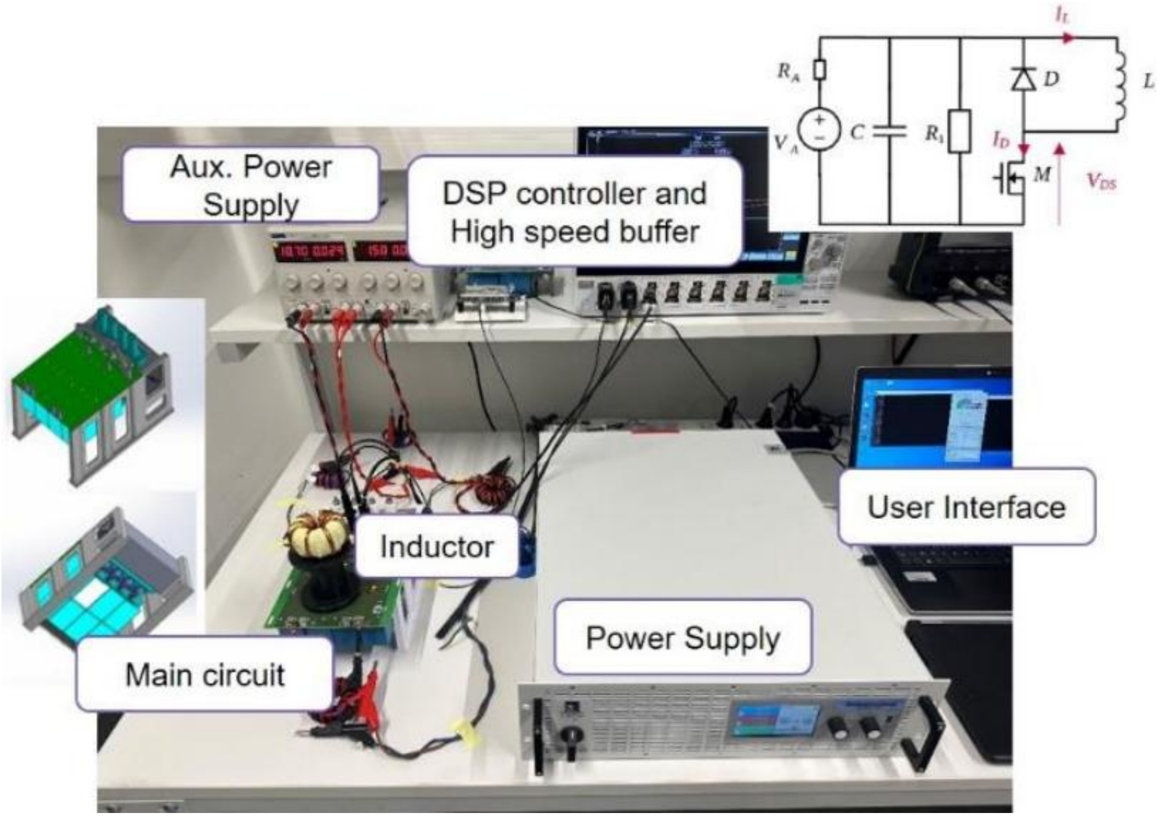
BNC tip adapter provides shielded connection



Flying lead tip adapter creates a large loop, coupling in noise and altering frequency response

Isolation and Ground Loops

- High voltage testing requires attention to safety
- Ensure all equipment is used within its safety ratings
- **Do not** “float” the scope to address common-mode challenges
- Fast switching circuits create “ground shifts”
  - A common net on a schematic does not guarantee points are at the same voltage dynamically
  - High dv/dt and di/dt results in dynamic voltage differentials on the same net
- Parasitic capacitors are everywhere!



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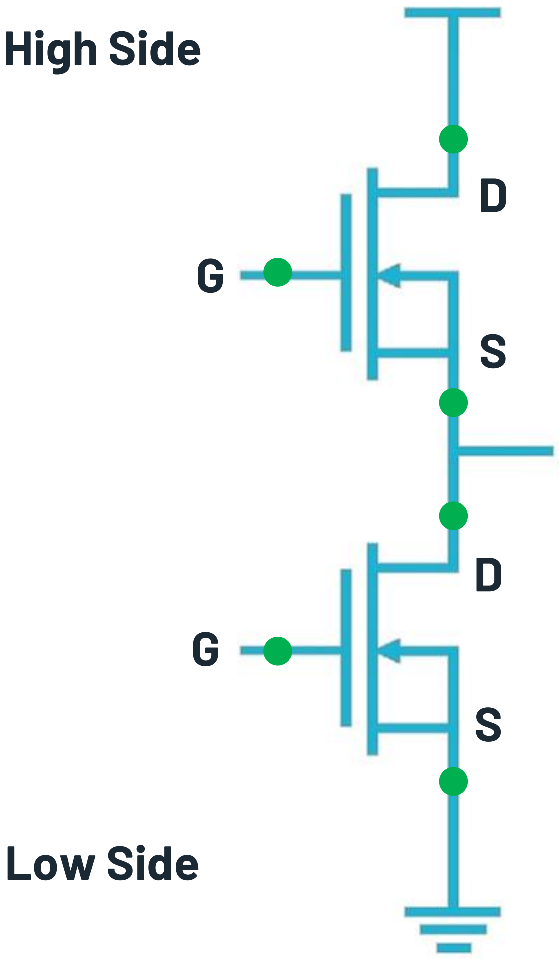
[1] “Mission-Profile-Related Evaluation of the Threshold-Voltage Stability of SiC MOSFETs”, CIPS 2024

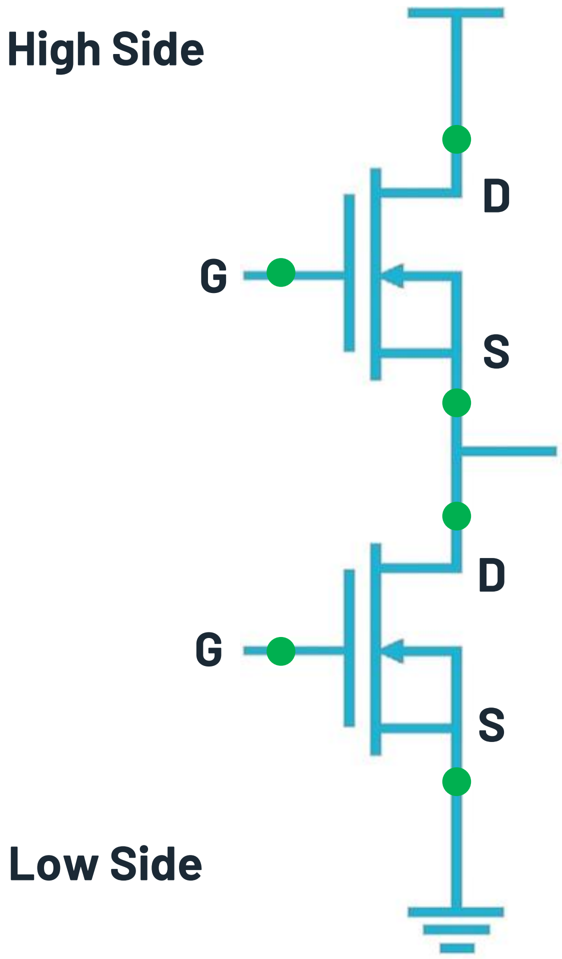
Top Probing Considerations

Top Probing Considerations



- Bandwidth
- Differential Voltage
- Common Mode Voltage
- Common Mode Rejection Ratio
- Loading
- Isolation

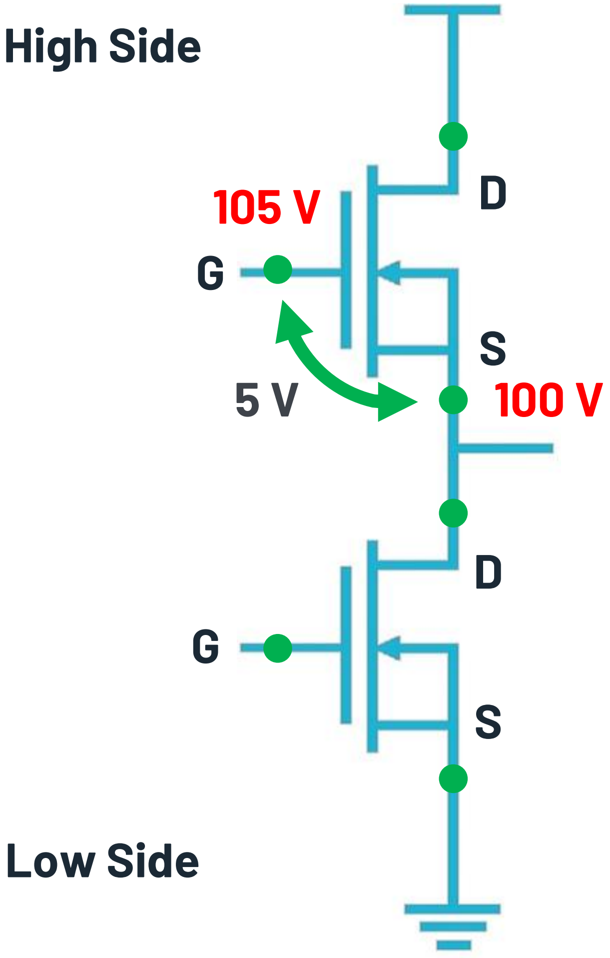
Top Probing Considerations



System Bandwidth

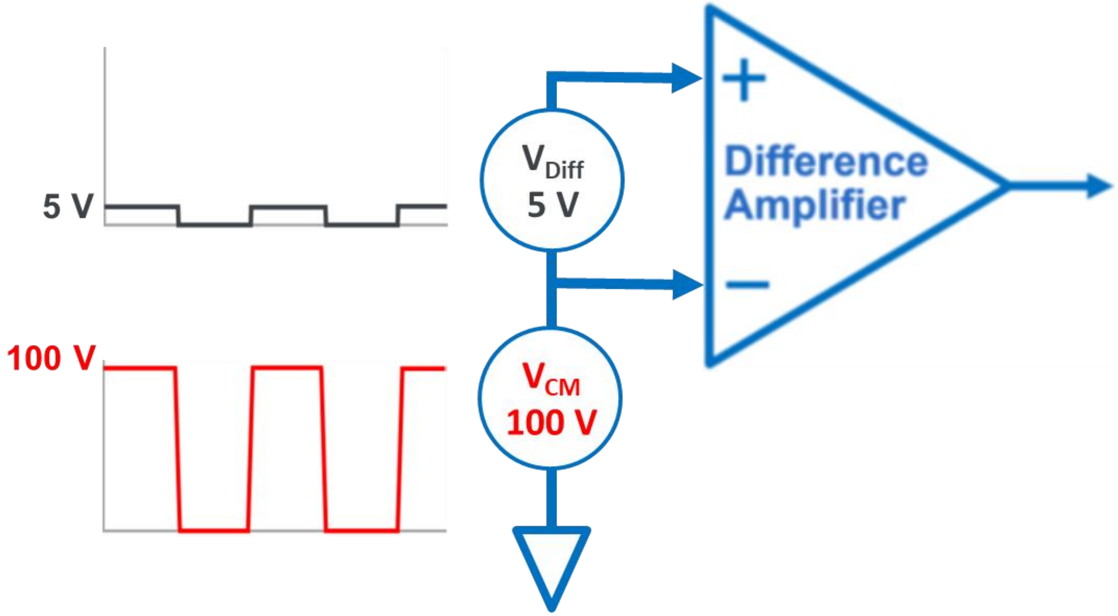
$$BW_{-3dB} = \frac{1}{\sqrt{\frac{1}{(BW_{-3dB,\ Scope})^2} + \frac{1}{(BW_{-3dB,\ Probe})^2}}}$$

Top Probing Considerations

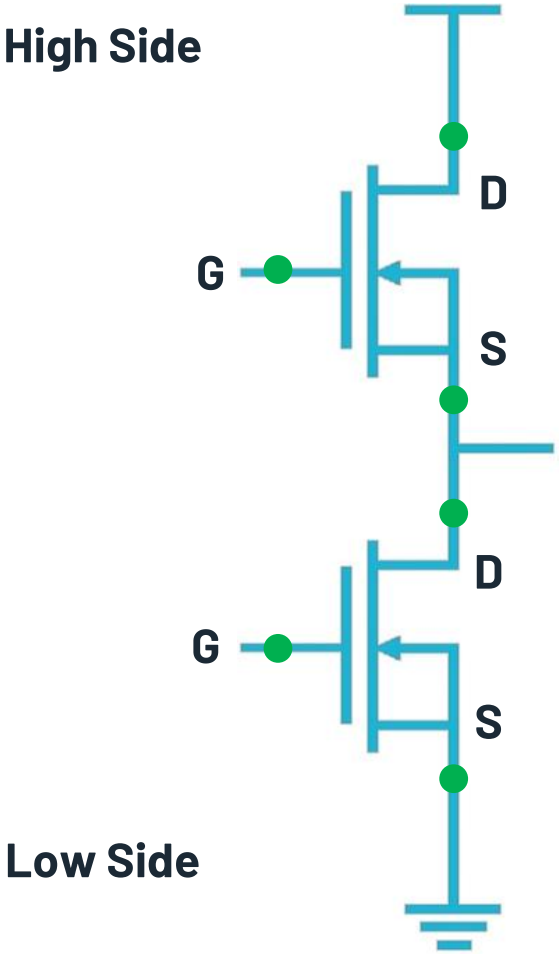


Differential Voltage

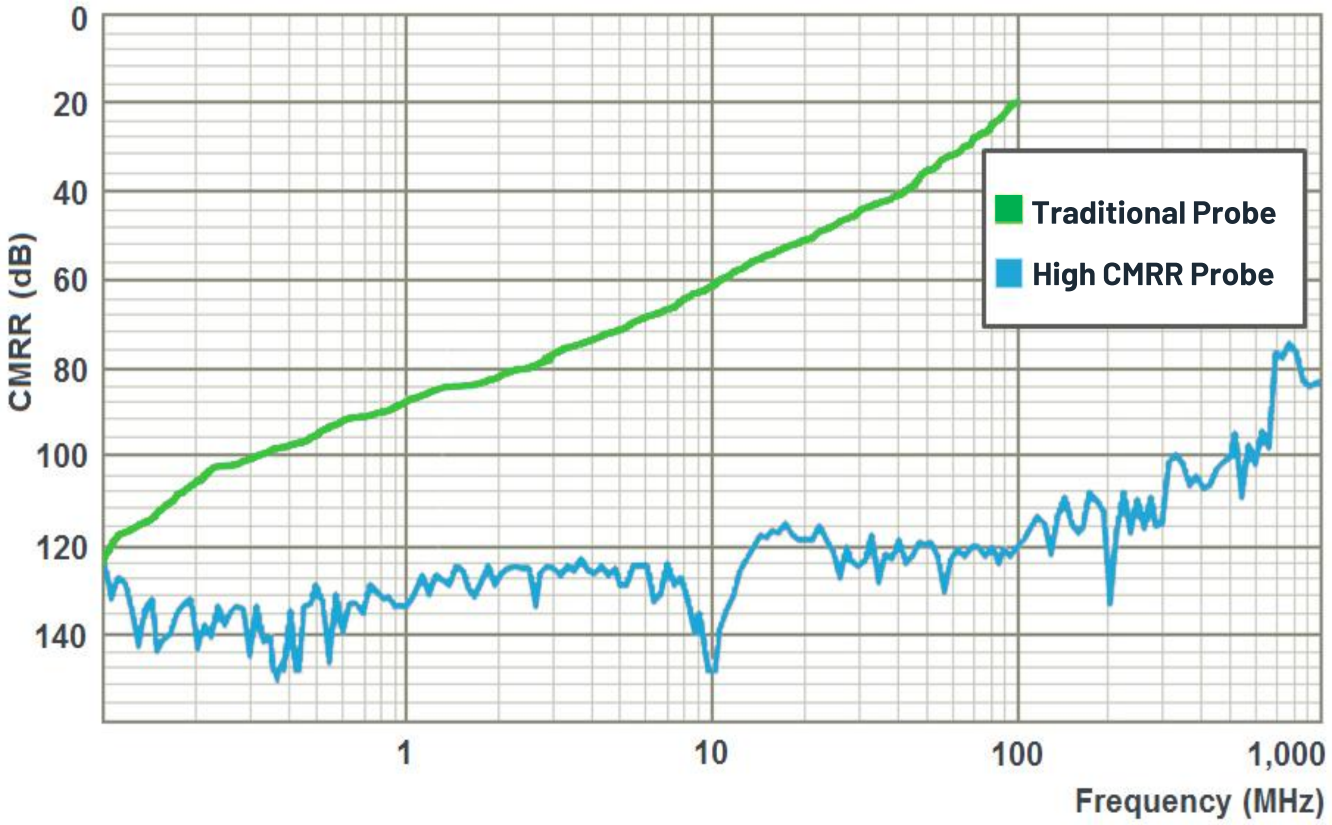
Common Mode Voltage



Top Probing Considerations

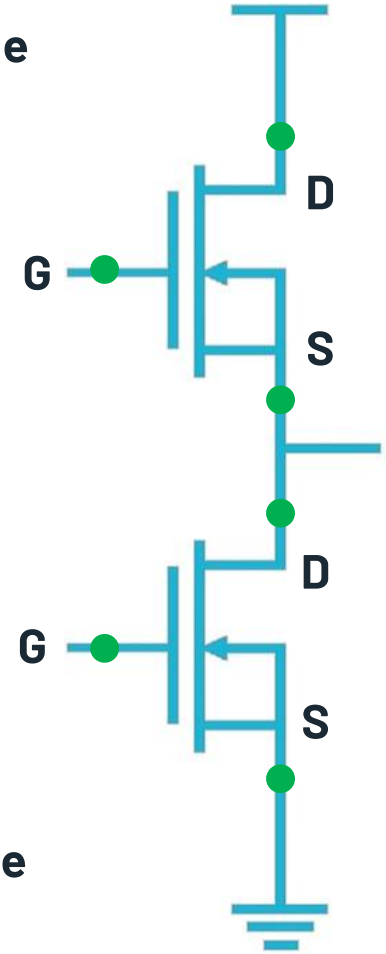


Common Mode Rejection Ratio



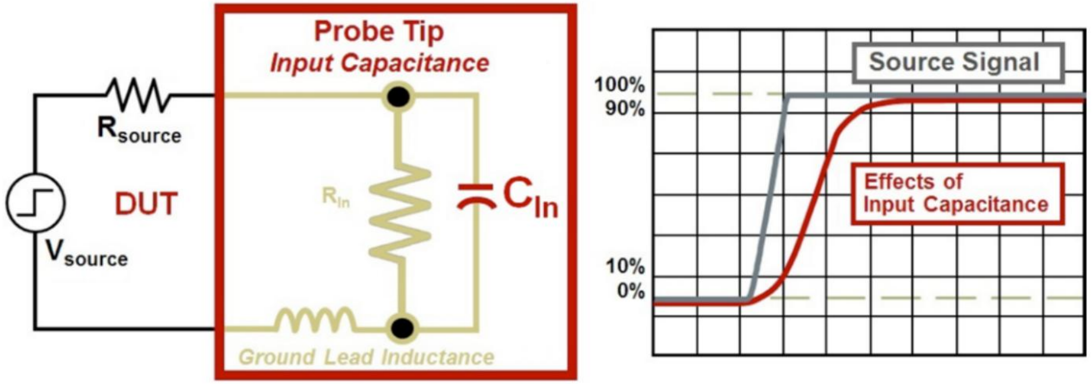
Top Probing Considerations

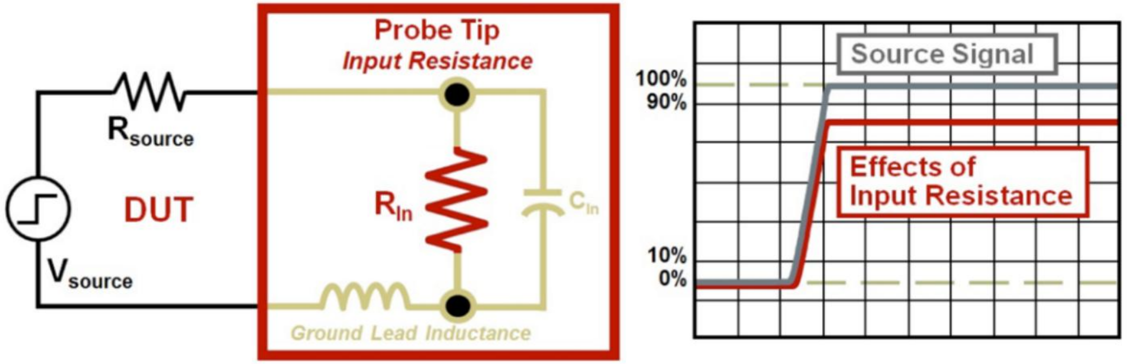
High Side



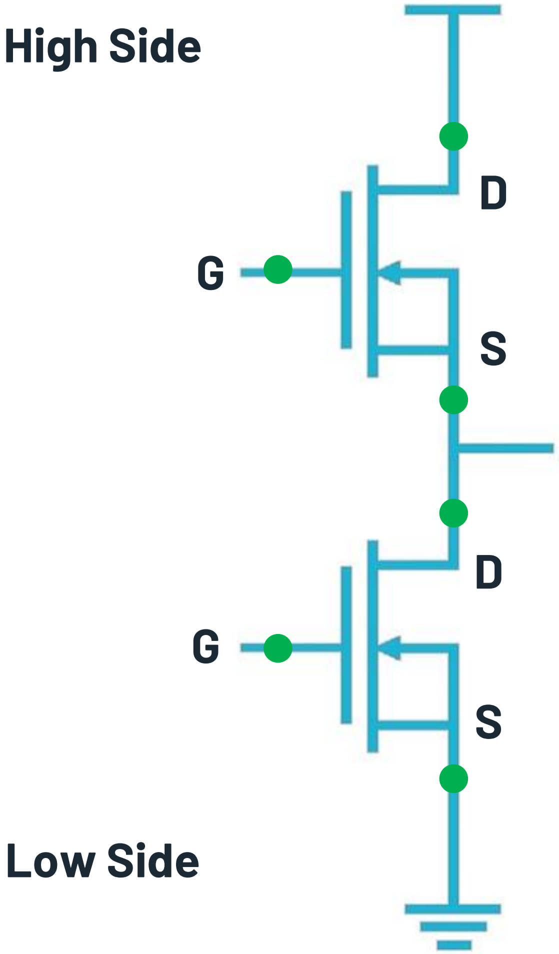
Low Side

Loading

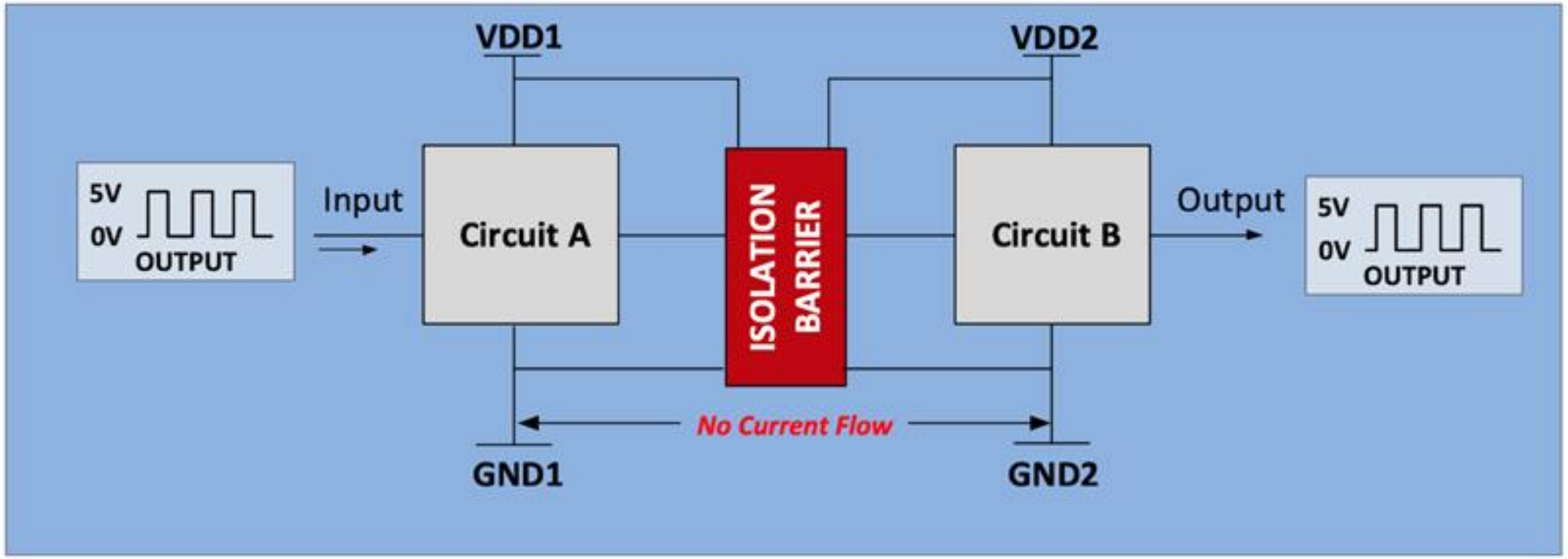




Top Probing Considerations



Isolation



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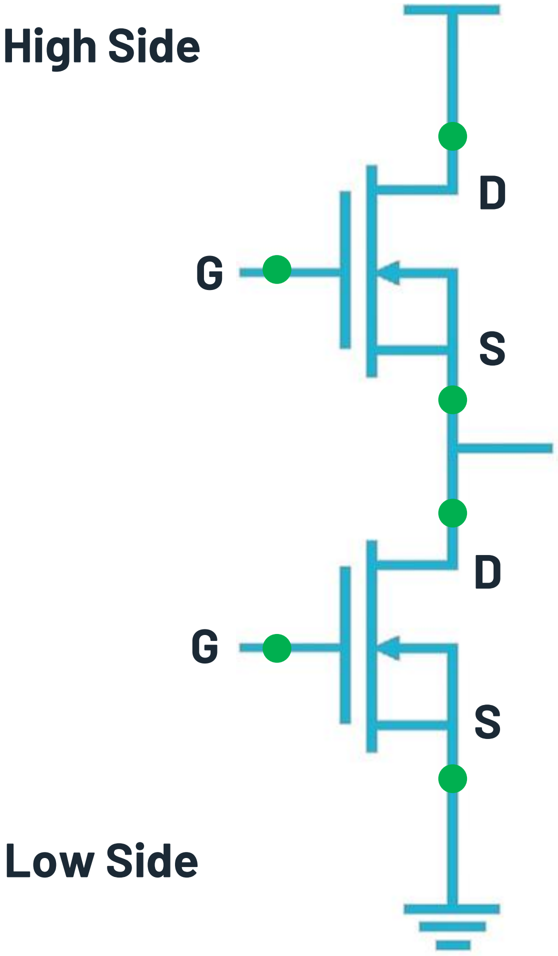
[1] https://www.powersystemsdesign.com/articles/improving-ev-safety-and-reliability-with-galvanic-isolation/22/14838

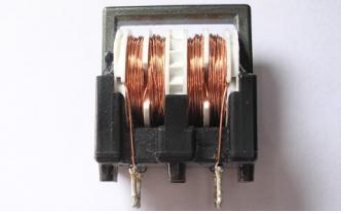
Top Probing Considerations



Current Measurement

Shunt Resistor

- Current measurements from DC to high frequencies AC
- Used e. g. for integrated sensors



Transformer

- Current measurements only for alternating currents (AC)
- Used e. g. for AC current probes

Hall Sensor

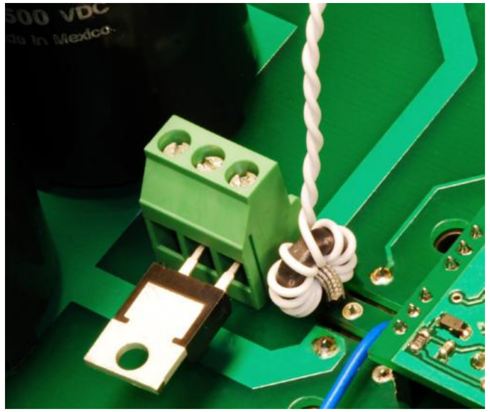
- Current measurements from DC to low frequencies AC
- Used e. g. for DC voltage sensors

Transformer + Hall-Sensor

- Current measurements from DC to high frequencies AC
- Used for typical current clamps

Two-stage Current Transformer

- Advantages
  - Isolated measurement, so current can be captured in devices not tied to the –DC bus
  - Lesser chance of common mode currents circulating between other measurement channels (V_{DS},V_{GS}) on oscilloscope
- Disadvantages
  - Only suitable for pulse measurements. Cannot capture currents in a running power converter (no DC)
  - Lower bandwidth than high-quality CVR (current viewing resistor)



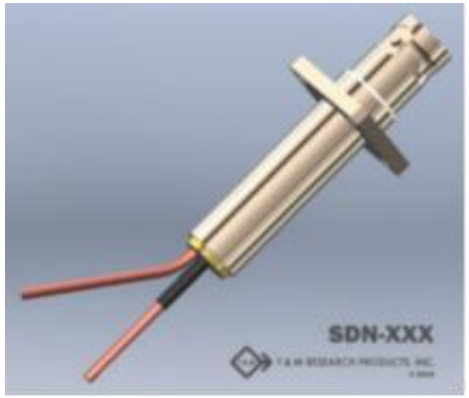
First Stage

Second Stage

Current Viewing Resistor (CVR)

- Advantages
    - Highest bandwidth of the three methods
    - Can be used in a running power converter, not just DPT

- Disadvantages
    - Non-isolated measurement, which limits it to devices tied to the – DC bus
    - The lack of isolation makes common mode currents circulating between the channels an issue, which must be mitigated to avoid offsets and error
    - More difficult to integrate into layout without disturbing the layout current loop

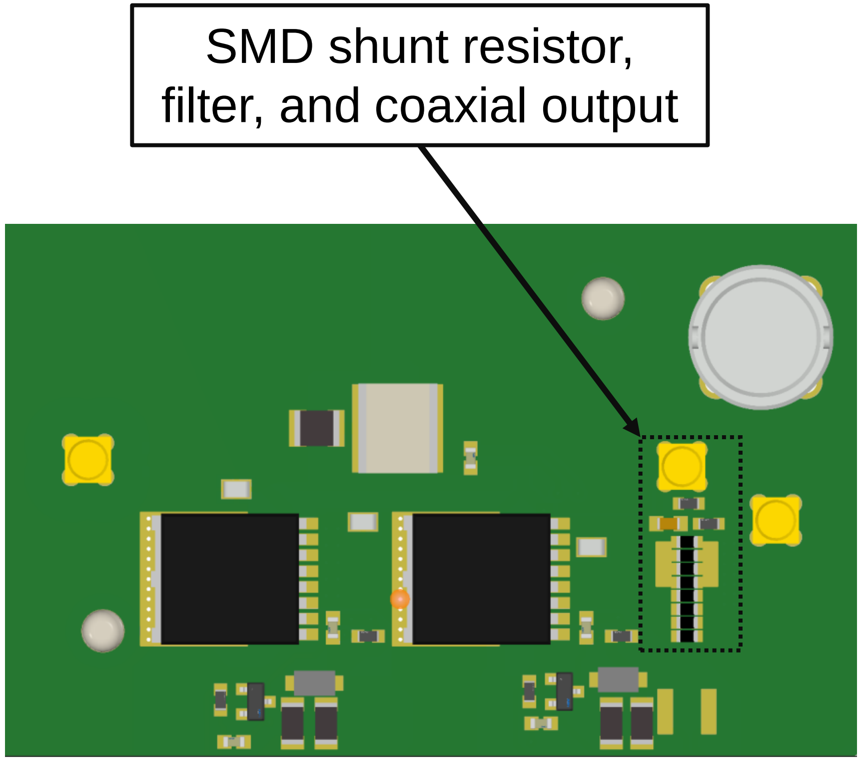


Coaxial CVR

Surface Mount Shunt Resistors

- Advantages
  - Capable of high bandwidth and accuracy
  - Least expensive of all solutions
  - Least insertion inductance

- Disadvantages
  - Requires proper filtering to mitigate the effects of parasitic inductance
  - Performance is very dependent on layout
  - Power limited by package size

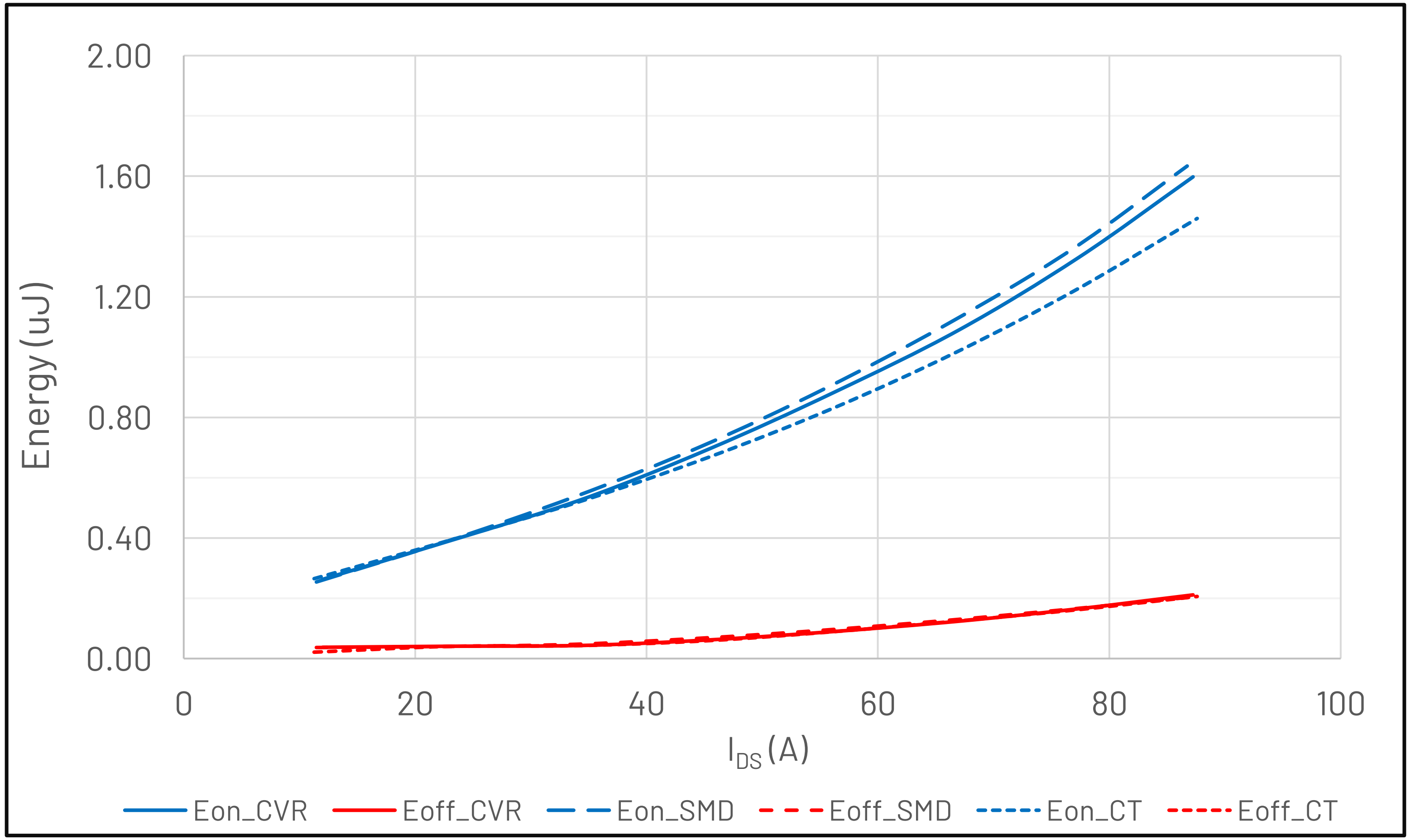


SMD shunt resistor, filter, and coaxial output

Half bridge with SMD resistor shunt measuring lower MOSFET I_{DS}

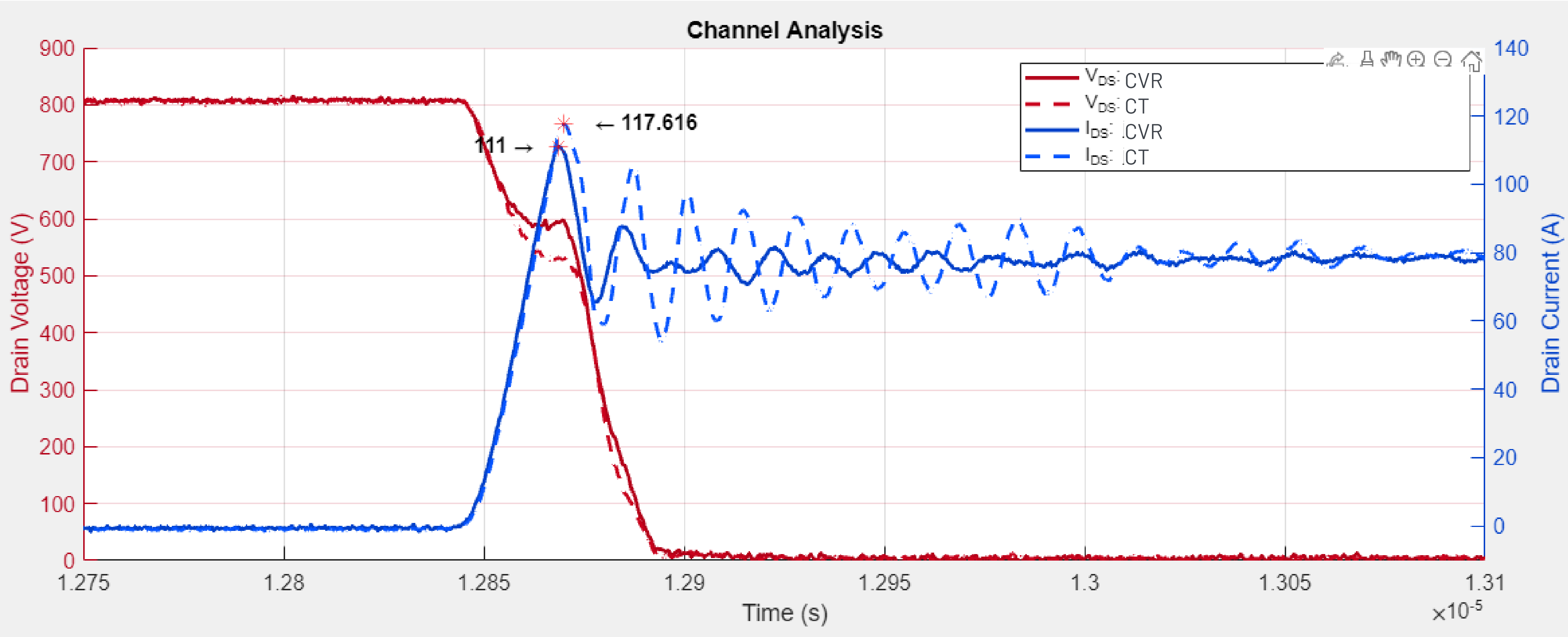
Switching Energy Compared Using Different Current Sensors

Conditions:
T_{vj} = 25°C
V_{DD} = 800V
$R_{G(ext)}$ = 2.5Ω
V_{GS} = -3V/+15V
FWD = body diode
L = 64µH



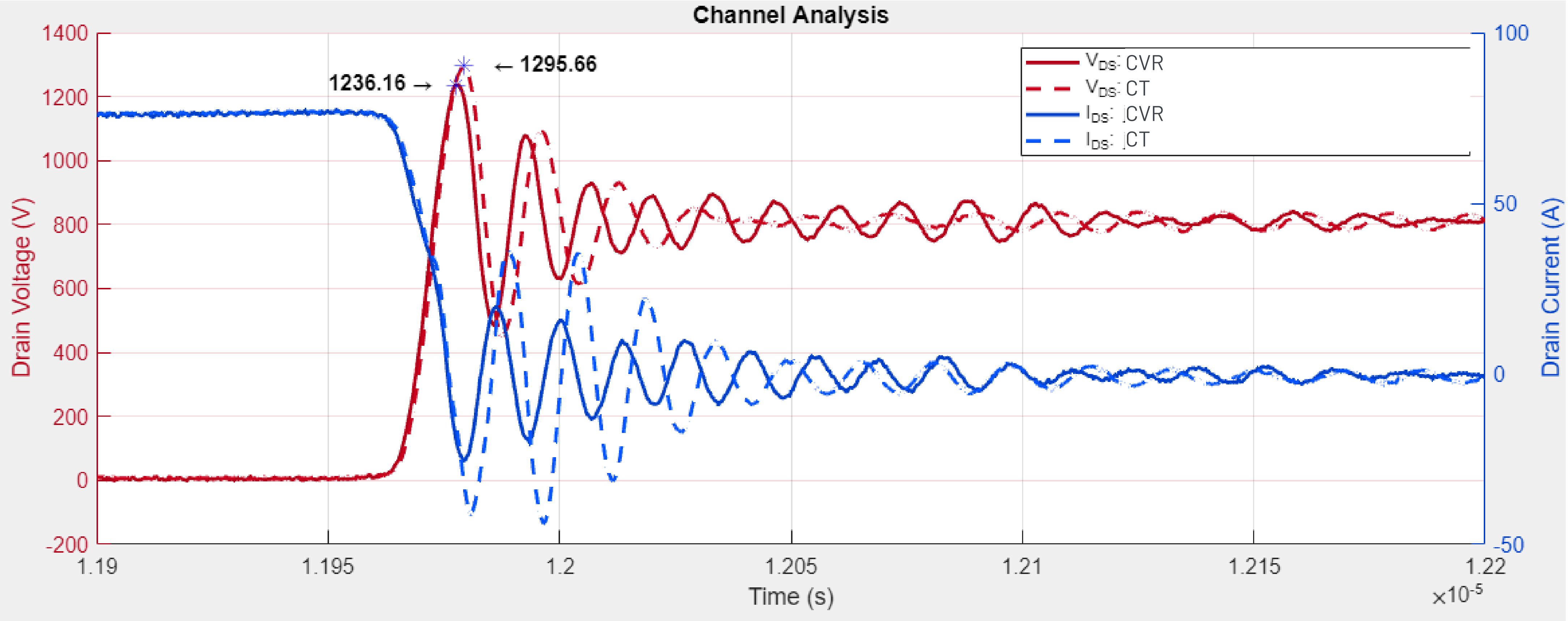
All three methods produce similar measurements. The CT shows slightly lower turn-on losses than the other two sensors.

Turn-on Waveforms (CVR vs. Pearson CT)



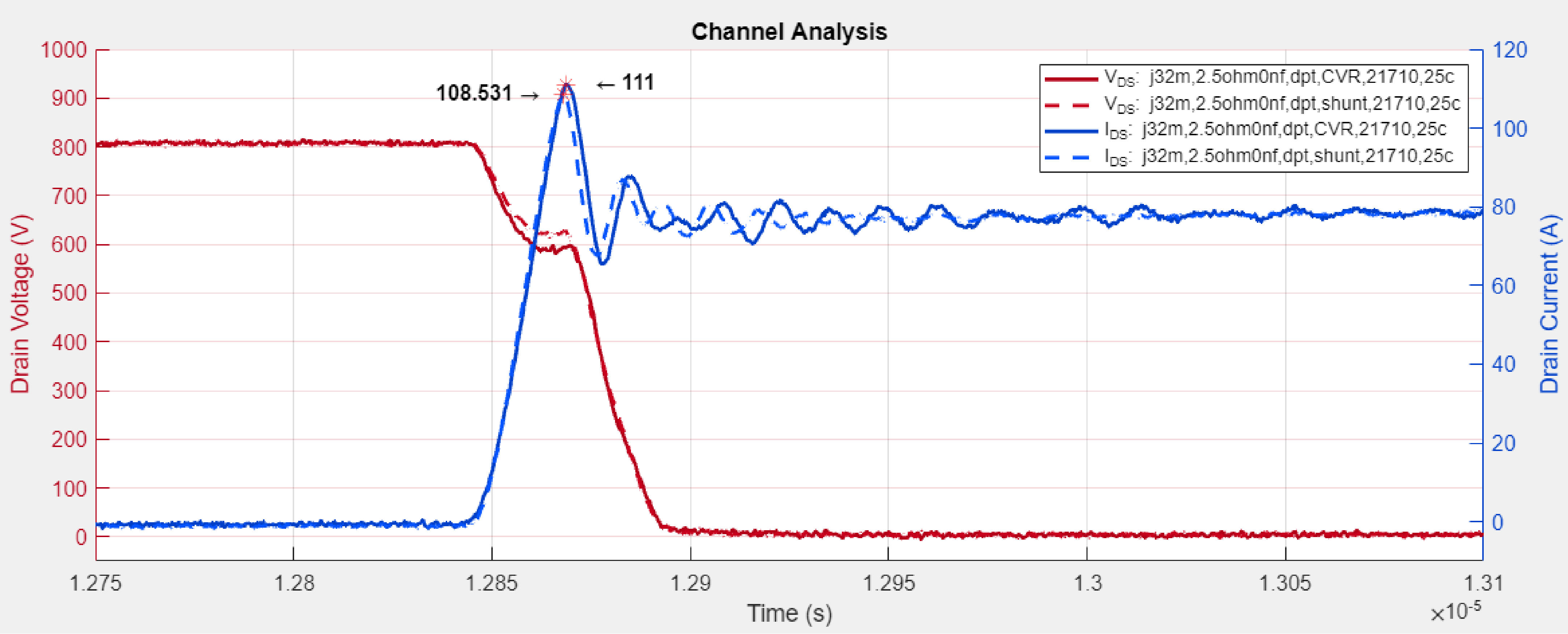
The CT adds more stray inductance to the loop which causes more ringing.

Turn-off Waveforms (CVR vs. Pearson CT)



The CT adds more stray inductance to the loop which causes more ringing.

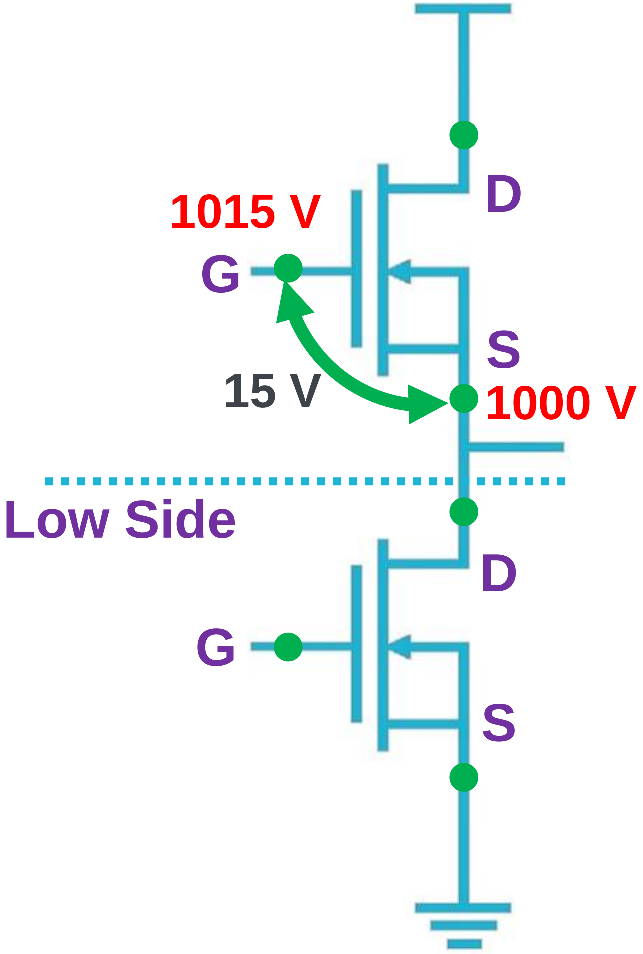
Turn-on Waveforms (CVR vs. SMD Shunt)



The SMD shunt shows very good matching with the T&M CVR (current viewing resistor)

Probing Recommendations

High Side VGS



	Isolated	Isolated	High Voltage Differential
	TIVP1	TICP1	THDP0200
Bandwidth	DC to 1 GHz	DC to 1 GHz	DC to 200 MHz
Maximum Measurement Voltage	±1.5kV differential	±50V differential	±1.5kV differential
Common Mode Voltage	60,000 V	1,800 V	±1,500 V
Loading (input + to -)	40 MΩ ǁ <2.4 pF (tip dependent)	5 kΩ ǁ <3 pF (tip dependent)	10 MΩ ǁ <2 pF
Aberrations	Good	Great	Better
Isolation	Optical	RF	None
Common Mode Rejection Ratio	-160 dB (100M:1)	-140 dB (100M:1)	>-80 dB (10k:1)
CM Error (1kV) @ DC	1 mV	178 mV	0.1 V
CM (1kV) @1 MHz	1 mV	3.16 V	3.2 V
CM Error (1kV) @100 MHz	1 mV	5.62 V	45.2 V
CM Error (1kV) @ Full BW	0.1 V	50 V	178.6 V
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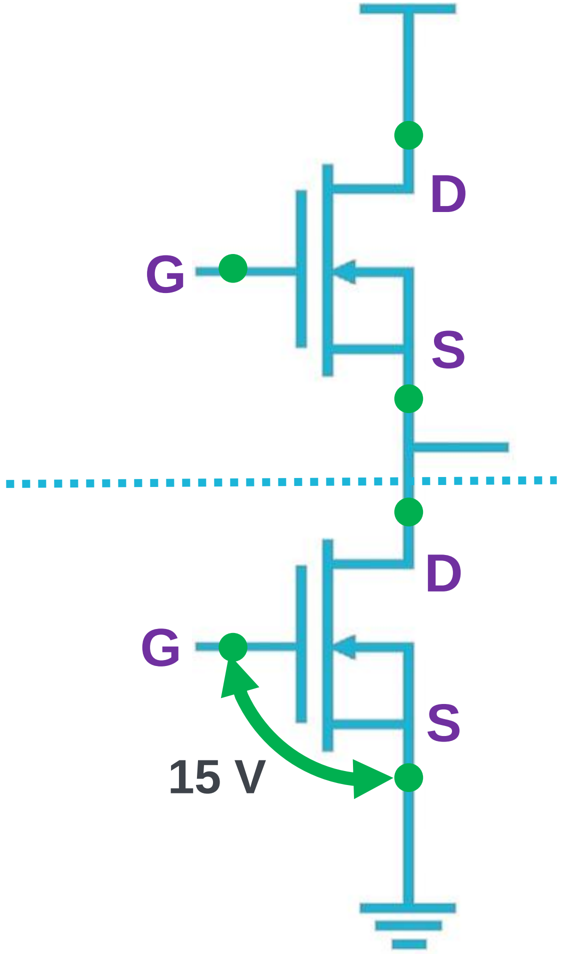
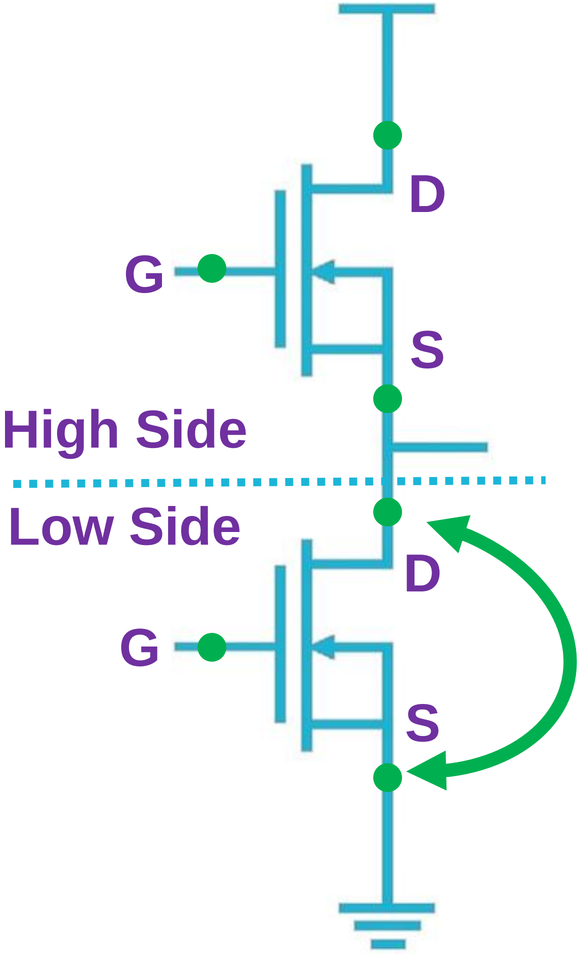
Low Side VGS



	Single Ended	High Voltage Differential	Isolated
	TPP0850 / TPP1000	THDP0200	TIVP1
Bandwidth	800 MHz / 1 GHz	DC to 200 MHz	DC to 1 GHz
Maximum Measurement Voltage	2.5kVpk, 1kV CAT II / 300V CAT II	±1.5kV differential	±1.5kV differential
Common Mode Voltage	N/A	±1,500 V	60,000 V
Loading (Input + to ground)	50 MΩ ‖ <1.8 pF / 10 MΩ ‖ <4 pF	5 MΩ ‖ <4 pF	None
Loading (Input – to ground)	N/A	5 MΩ ‖ <4 pF	<5 pF
Loading (input + to -)	N/A	10 MΩ ‖ <2 pF	40 MΩ ‖ <2.4 pF (tip dependent)
Aberrations	Best	Better	Good
Isolation	None	None	Optical
Common Mode Rejection Ratio	N/A	>-80 dB (10k:1)	-160 dB (100M:1)

● ● ●

Low Side VDS



	Single Ended	High Voltage Differential	Isolated
	TPP0850 / TPP1000	THDP0200	TIVP1
Bandwidth	800 MHz / 1 GHz	DC to 200 MHz	DC to 1 GHz
Maximum Measurement Voltage	2.5kVpk, 1kV CAT II / 300V CAT II	±1.5kV differential	±1.5kV differential
Common Mode Voltage	N/A	±1,500 V	60,000 V
Loading (input + to -)	N/A	10 MΩ ‖ <2 pF	40 MΩ ‖ <2.4 pF (tip dependent)
Aberrations	Best	Better	Good
Grounding			
Isolation	None	None	Optical
Common Mode Rejection Ratio	N/A	>-80 dB (10k:1)	-160 dB (100M:1)

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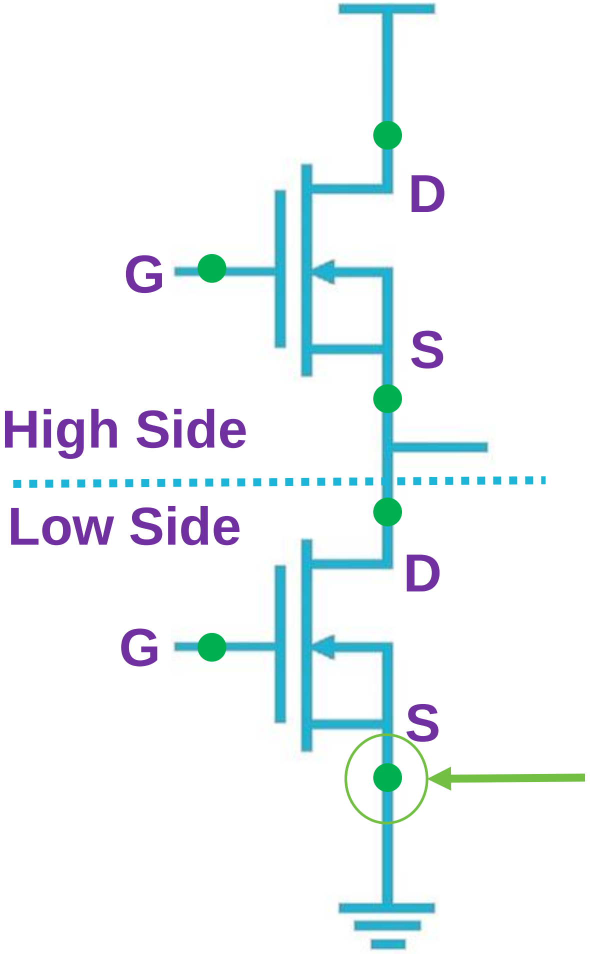
Low Side ID

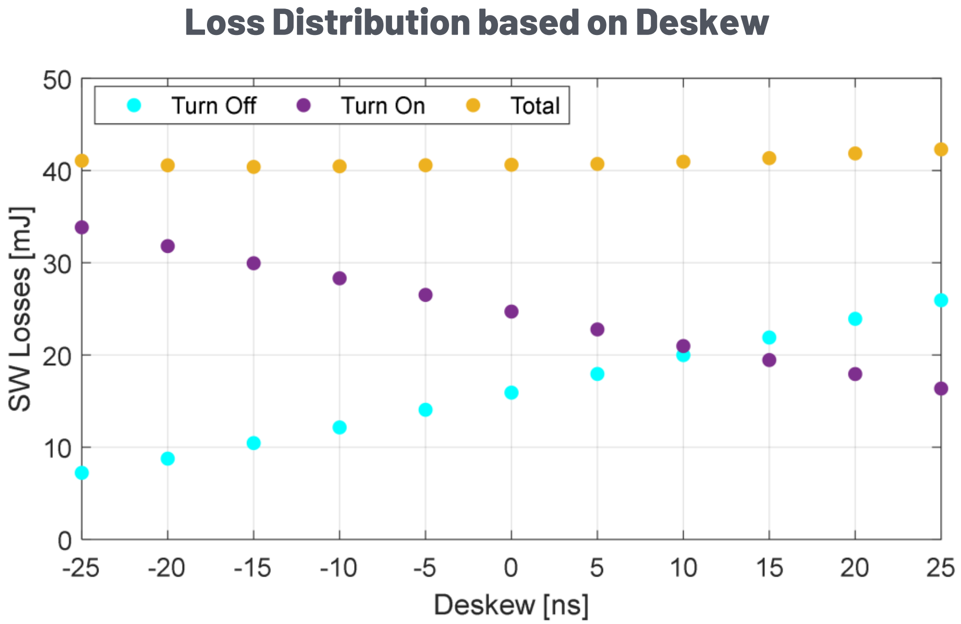


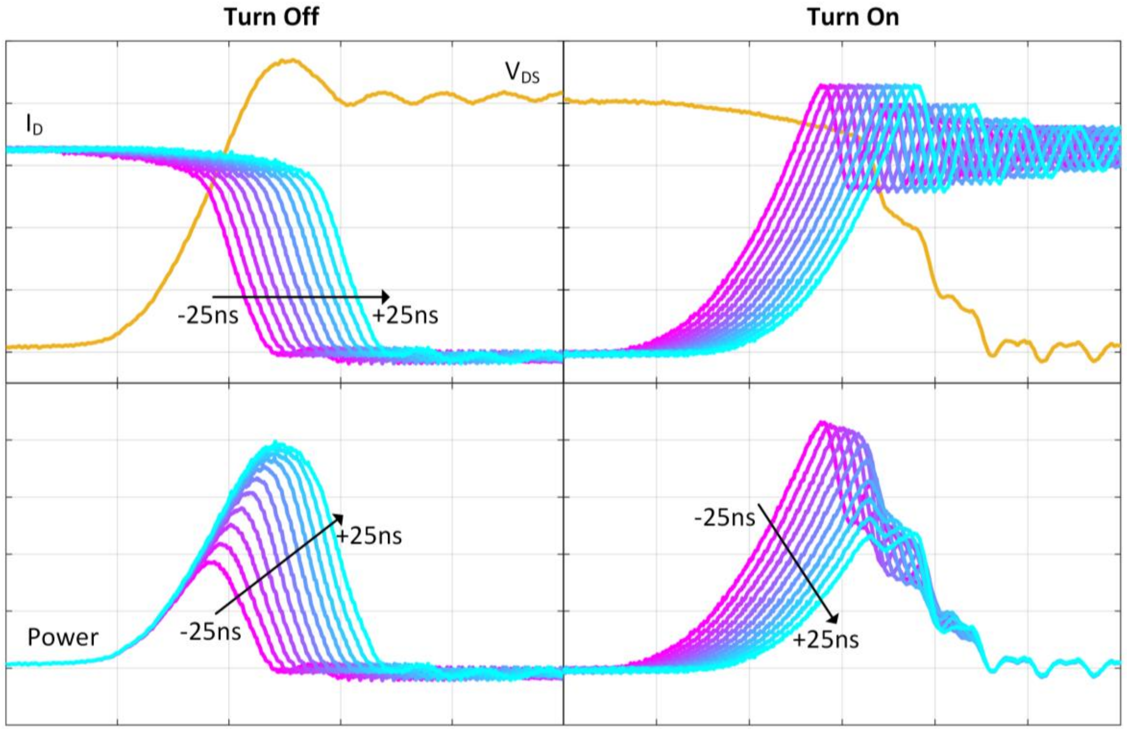
	Rogowski	Hall Effect	Isolated
	TRCP0060	TCP0030A	TICP100
Bandwidth	12 Hz – 30 MHz	DC to 120 MHz	DC to 1 GHz
Current Range	500 mA – 3kA peak	30 A RMS	13 mA – 1.3 kA
Isolation	Yes	Yes	RF
Common Mode Voltage	N/A	150 V CAT II	1,800V
Common Mode Rejection Ratio	N/A	>-80 dB (10Mk:1)	-140 dB (100M:1)
	●	●	●

De-Skew

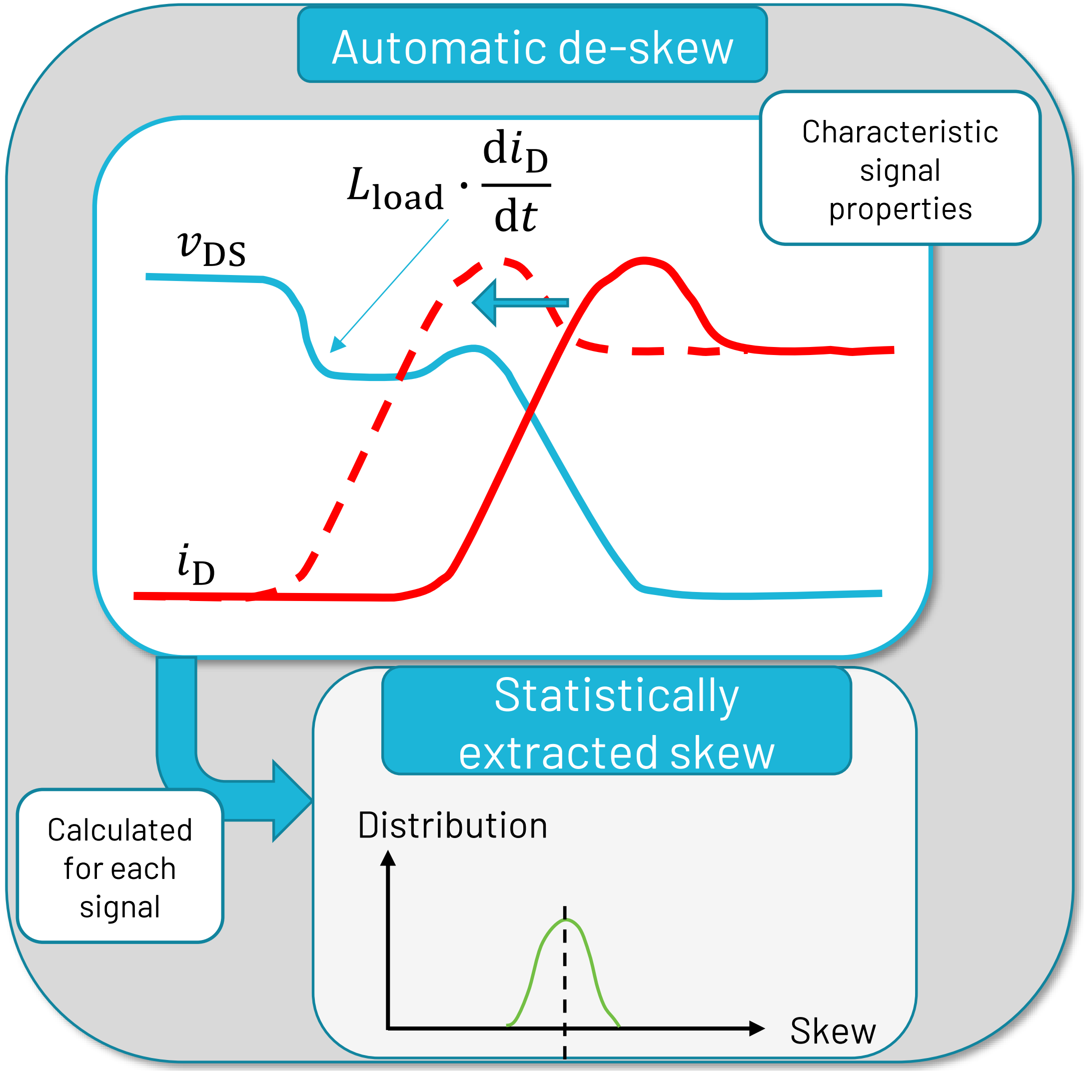
Accurate Calculation of Energies and timing highly dependent on deskew

- Loss distribution from E_{ON} to E_{OFF} can be skewed based on oscilloscope deskew setup





Automatic De-Skew

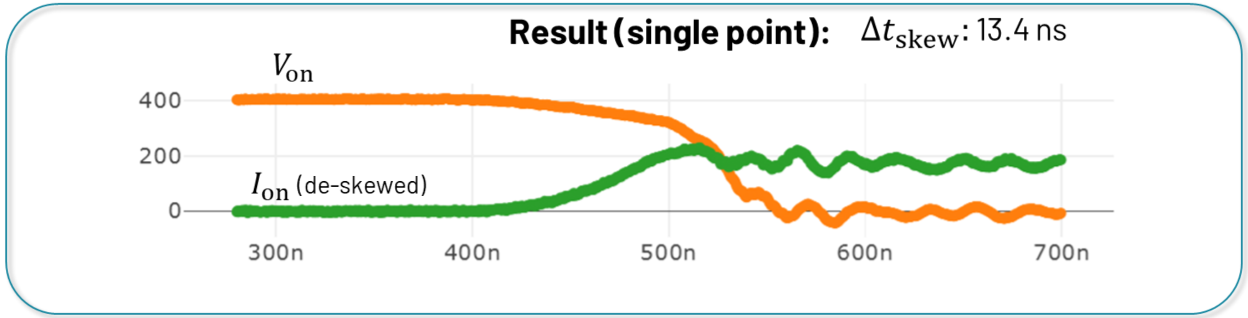


Characteristic signal properties

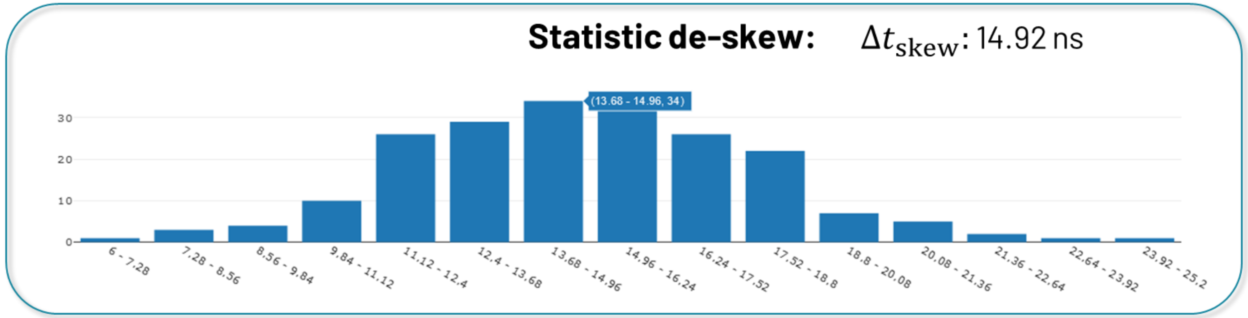
Calculated for each signal

Statistically extracted skew

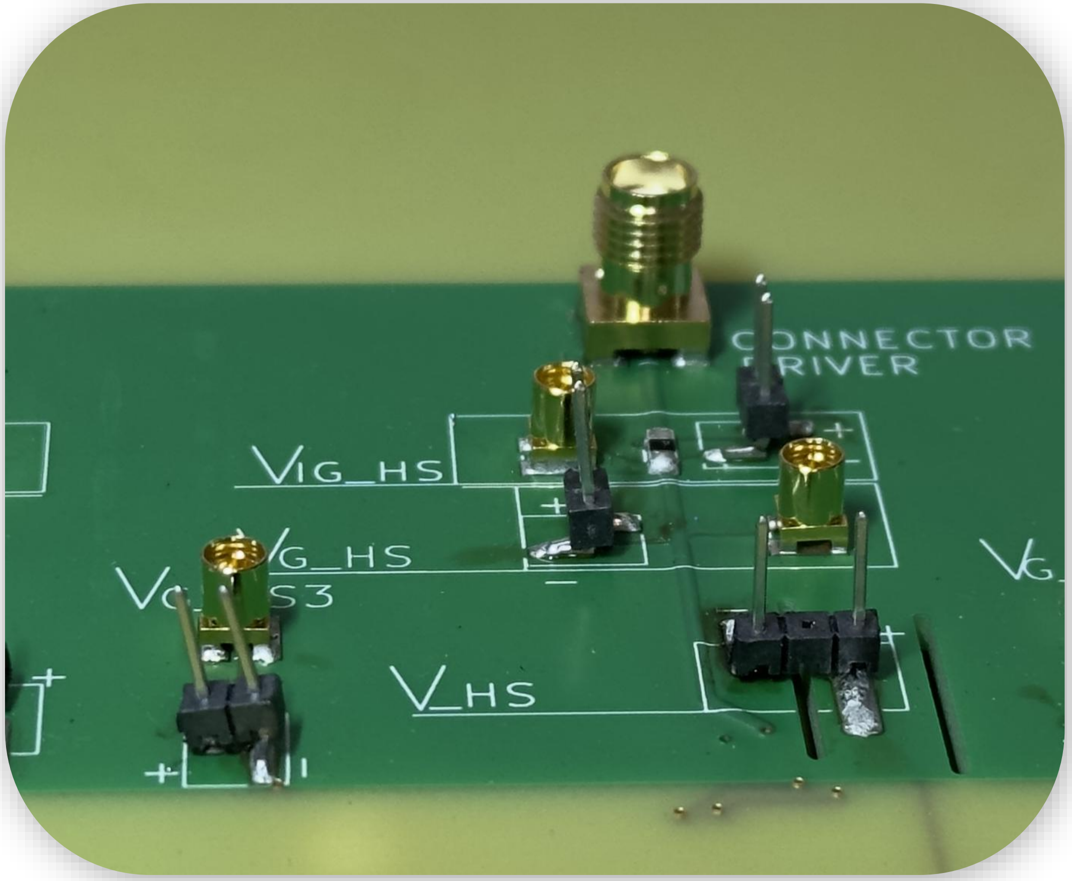
Result (single point): Δt_{skew}: 13.4 ns



Statistic de-skew: Δt_{skew}: 14.92 ns



How to Probe In-Circuit

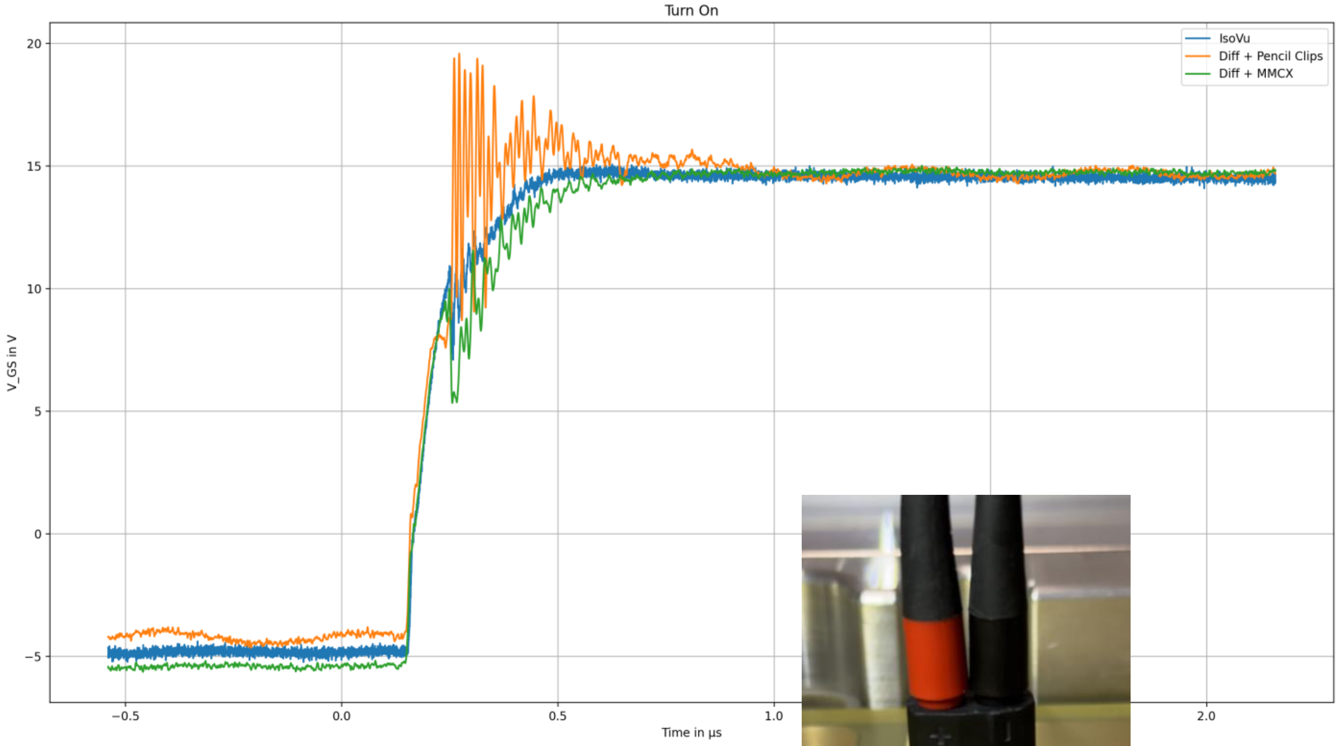


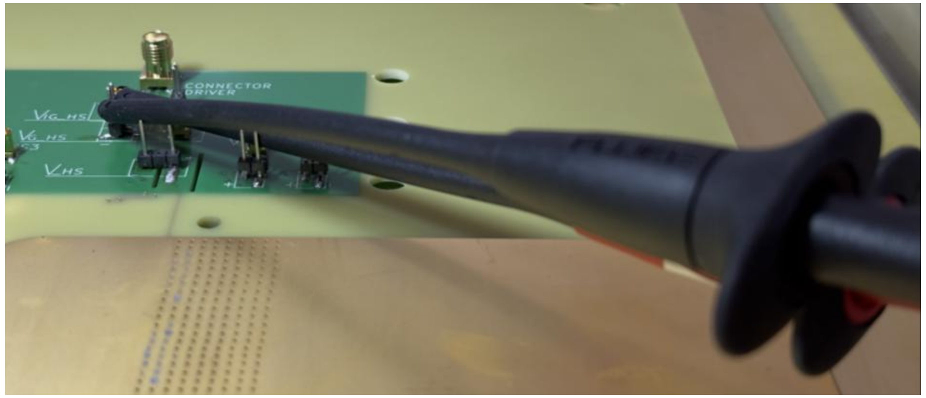
Probing Solutions

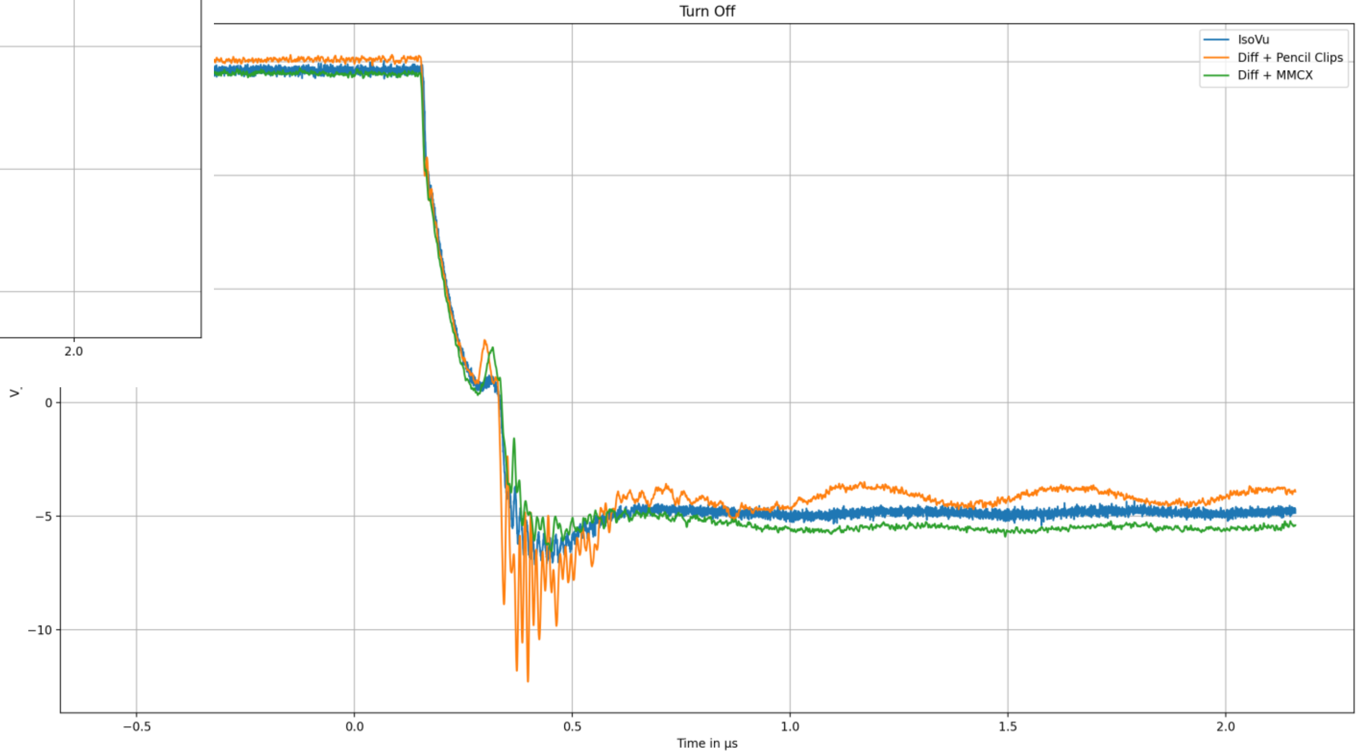
One circuit - different probe options

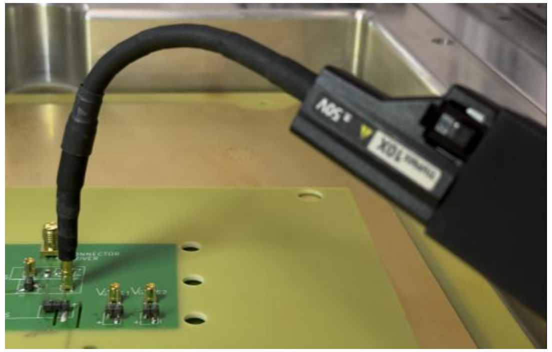
Select the probing solution (test pins) in accordance to your needs

How to Probe In-Circuit

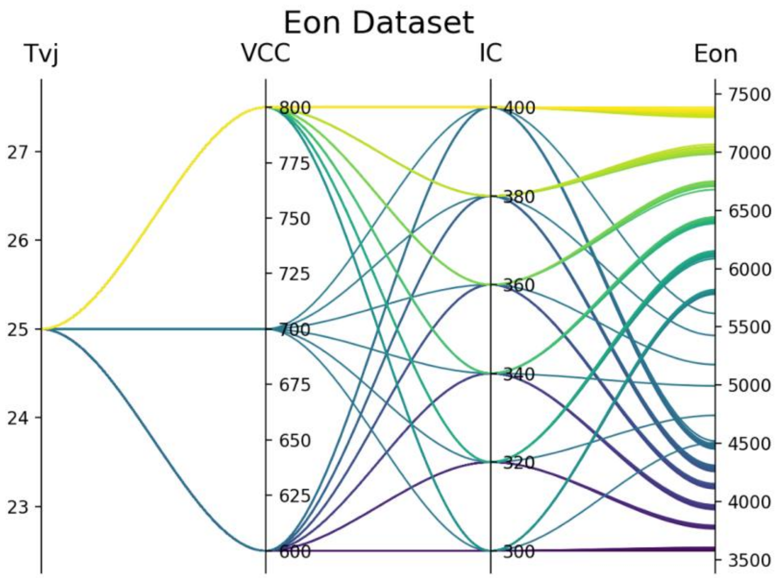


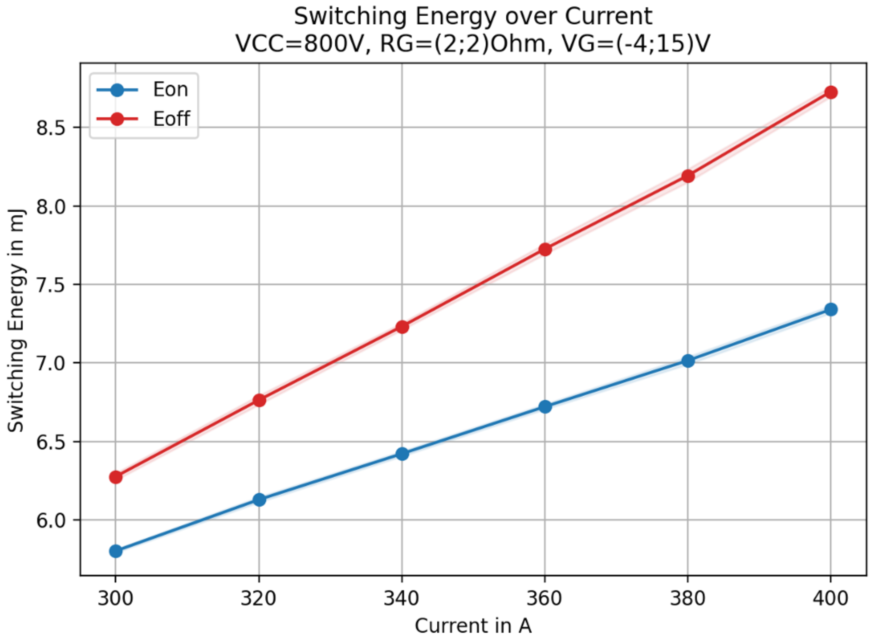


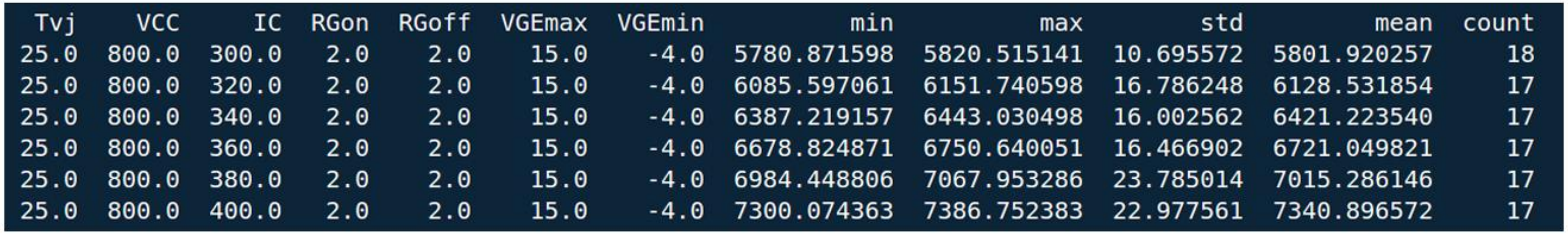




Uncertainty

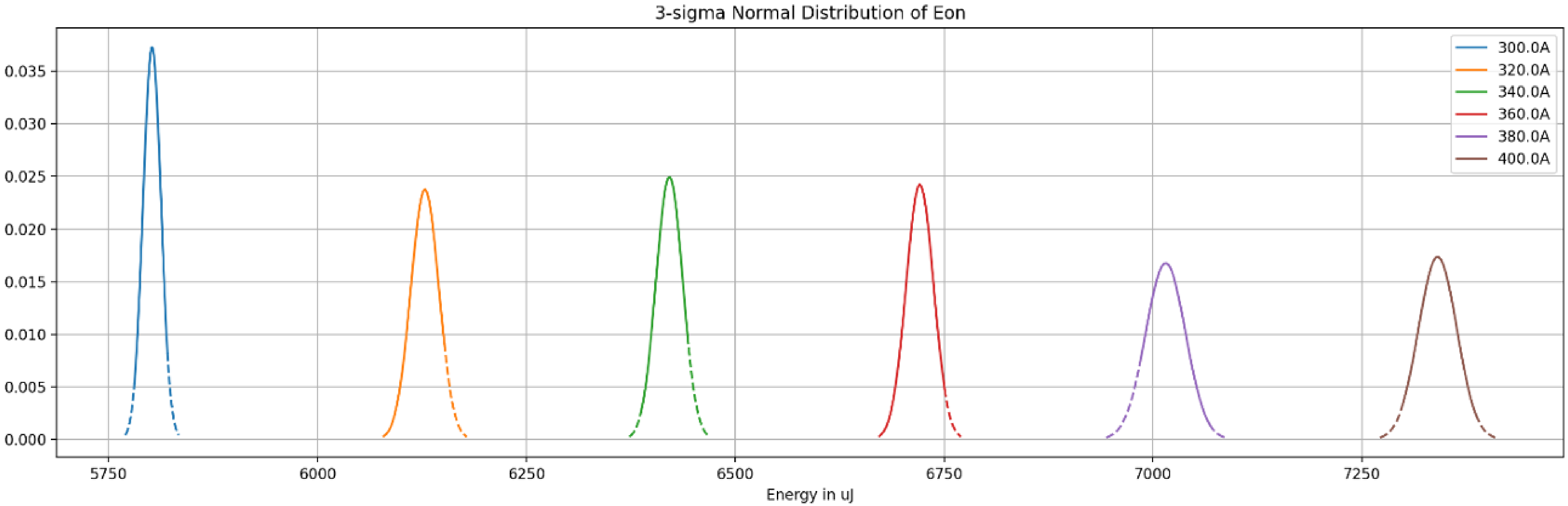






```
 Tvj    VCC     IC  RGon  RGoff  VGEmax  VGEmin          min          max        std         mean  count
25.0  800.0  300.0   2.0    2.0    15.0    -4.0  5780.871598  5820.515141  10.695572  5801.920257     18
25.0  800.0  320.0   2.0    2.0    15.0    -4.0  6085.597061  6151.740598  16.786248  6128.531854     17
25.0  800.0  340.0   2.0    2.0    15.0    -4.0  6387.219157  6443.030498  16.002562  6421.223540     17
25.0  800.0  360.0   2.0    2.0    15.0    -4.0  6678.824871  6750.640051  16.466902  6721.049821     17
25.0  800.0  380.0   2.0    2.0    15.0    -4.0  6984.448806  7067.953286  23.785014  7015.286146     17
25.0  800.0  400.0   2.0    2.0    15.0    -4.0  7300.074363  7386.752383  22.977561  7340.896572     17
```

Uncertainty



Summary

- SiC is now a mainstream power semiconductor technology
- Faster switching speeds require more careful measurement techniques and proper equipment
- Accurate measurements are necessary to properly characterize devices and optimize systems
- Isolated probes provide very high CMMR allowing for accurate gate voltage measurements
- High bandwidth voltage probes and current sensors are required to accurately capture dynamic behavior
- Following the recommendations outlined here will make designing with SiC fast and easy

Deep-Dive Webinar Series – Measure the Change

EXPLORE THE TEST EQUIPMENT, TECHNIQUES, AND MEASUREMENTS TO OPTIMIZE YOUR SIC DESIGN

Part 2

Section 1: Getting Started with Device Level Testing
- ☐ Test configuration and probe setup
- ☐ Understanding JEDEC definitions

Section 2: Tools and Platforms
- ☐ Evaluation platforms: setup and features
- ☐ SpeedVal demo overview
- ☐ Using module CIL boards

Section 3: Key Test Techniques – Interpreting Test Results
- ☐ Double Pulse Testing (DPT)
- ☐ Body Diode Reverse Recovery (Qrr)
- ☐ Measuring Vds Overshoot
- ☐ Cross Talk Analysis

Section 4: Device Optimization – Using Data to Optimize Performance
- ☐ Tuning Gate Resistance (Rg) and Capacitance (Cg)
- ☐ Optimizing Device Performance

Part 3

Section 1: Designing for Testability
- ☐ Test points and low-cost connection methods
- ☐ Ensuring Rogowski coil accessibility

Section 2: Optimizing Device & Circuit Performance
- ☐ Managing Vds and Vgs transient overshoots
- ☐ Adjusting gate resistance (Rg)
- ☐ Improving loop inductance
- ☐ Gate drive layout: reducing coupling to high dv/dt nodes

Section 4: Improving Current Distribution & Symmetry
- ☐ Ensuring balanced Ids sharing in parallel devices
- ☐ Using symmetrical layouts for improved efficiency
- ☐ Balancing inductors
- ☐ Proper gate drive circuit design with Rks for parallel devices

Section 4: Reliability and Thermal Management
- ☐ Thermal measurements to validate current sharing
- ☐ SOA validation

https://tek.brandlive.com/Si-to-SiC/en

THANK YOU

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